

**NEW YORK CITY COLLEGE OF TECHNOLOGY**  
**The City University of New York**

**DEPARTMENT:** Electrical Engineering Technology

**SUBJECT CODE:** EET2162

**AND TITLE:** Digital Electronics I

**COURSE DESCRIPTION:** Fundamental of digital electronics using Boolean algebra, truth tables, Karnaugh maps and waveforms to analyze and understand digital logic circuit design. Logic gates (AND, OR, NOR, EX-OR), binary arithmetic, flip-flops, counters and registers are analyzed in experiments.

**PREREQUISITES:** EET1240, EET1241

**TEXTBOOK:** Digital Systems Principles and Applications 11<sup>th</sup> Ed.  
By Tocci, Widmer, and Moss - Prentice Hall 2013

**COURSE OBJECTIVES/  
COURSE OUTCOMES:** Upon completion of this course students will be able to:

1. Analyze and design combinatorial logic circuits with multiple inputs or outputs (ETAC/ABET Criteria, 3.1, 3.4, 3.5, PC a)
2. Use Boolean algebra and Kmapping to reduce logic hardware to a minimum number of gates. (ETAC/ABET Criteria, 3.1, 3.5).
3. Convert logic circuits to NAND or NOR logic equivalent. (ETAC/ABET Criteria, 3.1, 3.4, 3.5, PC a).
4. Analyze and design arithmetic circuits. (ETAC/ABET Criteria, 3.1, 3.4, 3.5, PC a).
5. Analyze and design sequential logic circuits with multiple inputs/outputs (ETAC/ABET Criteria, 3.1, 3.4, 3.5, PC a).
6. Analyze and design counters and registers (ETAC/ABET Criteria, 3.1, 3.4, 3.5, PC a).

**TOPICS:** Topics include analysis, design implementation, and testing of basic combinatorial and sequential logic circuits: Boolean algebra and Karnaugh mapping techniques are covered to reduce redundant hardware.

**CLASS HOURS:** 2  
**LAB HOURS:** 3  
**CREDITS:** 3

**Updated by:** Professor Aron Goykadosh Spring - 2022  
**Coordinator:** Professor Aron Goykadosh  
Email: Agoykadosh@citytech.cuny.edu

**EXPERIMENTS**  
**ET2162**

**WEEK**

1	Orientation, Pulse Measurements and MultiSim applications
2	Logic Gates: AND, OR, NAND, NOR and Inverter Circuits.
3	Pilot Ejection and 3 Voter Problem - Using the DIGIAC.
4	Binary-Decimal and Decimal-Binary Decoders using the DIGIAC.
5	Combinational Lock using the DIGIAC.
6	Automatic Control using the DIGIAC.
7	Flip-Flops, Counting Circuits and Displays using the DIGIAC.
8	Combinational Logic using the SN7400 and DIGIAC Designer.
9	Mid-Semester Exam.
10	Combinational Logic SN7400 (continued).
11	Sequential Logic using the 7476 and DIGIAC Designer.
12	Counters using the SN7490.
13	Counters, Drivers, and Displays (7490, 7447, CO8708).
14	SN 7486 EX-OR, Decoder, Multiplexer
15	Final Exam

**GRADING POLICY:**

Homework and class participation	20%
Exams	20%
Midterm Exam:	15%
Lab Reports	15%
Final Exam	30%

<u>Letter Grade</u>	<u>Numerical Grade Ranges</u>	<u>Quality</u>
A	93-100	4.0
A-	90-92.9	3.7
B+	87-89.9	3.3
B	83-86.9	3.0
B-	80-82.9	2.7
C+	77-79.9	2.3
C	70-76.9	2.0
D	60-69.9	1.0
F	59.9 and below	0.0

<p style="text-align: center;"><b><u>Assessment</u></b></p> <p>The following assessment techniques are correlated to the course objectives as follows: In addition, each assessment technique incorporates one or more of the following ABET Criteria 3 and Criteria 5 outcomes (3.1, 3.4, 3.5, PC a).</p> <p><b><u>Course Objectives</u></b></p> <ol style="list-style-type: none"> <li>1. Analyze and design combinatorial logic circuits with multiple inputs/outputs.</li> <li>2. Use Boolean algebra and K Mapping to reduce logic hardware to a minimum.</li> <li>3. Convert logic circuits to NAND or NOR logic.</li> <li>4. Analyze and design arithmetic circuits.</li> <li>5. Analyze and design sequential logic circuits with multiple inputs/outputs.</li> <li>6. Analyze and design counters and registers.</li> </ol>	<p style="text-align: center;"><b><u>Assessment</u></b></p> <p>Given a truth table, the student will be able to:</p> <ol style="list-style-type: none"> <li>1.1 Write a SOP Boolean equation of the output.</li> <li>1.2 Sketch the circuit using logic gates.</li> <li>2.1 Reduce the hardware (number of gates) in (1.2) using Boolean algebra or KMapping techniques.</li> <li>3.1 Convert a combinatorial logic circuit with different gates to NAND logic only. 3.2 Convert a combinatorial logic circuit with different gates to NOR logic only.</li> </ol> <p>Given a truth table, the student will be able to:</p> <ol style="list-style-type: none"> <li>4.1 Analyze and design a full Adder.</li> <li>4.2 Analyze and design a full a Subtractor.</li> <li>5.1 Given a sequential circuit, the student will be able to: construct the state table, and state diagram of the circuit.</li> <li>6.1 Given a truth table, the student will be able to: analyze and design an up-counter, down counter, up- down counter, and shift register</li> </ol>
--	---

**Contribution of course to meeting the ETAC/ABET requirements, Criterion 5:**

EET2162 meets Criterion 5 by providing students with the knowledge to build, test, and apply digital electronic circuits. The course enables students to develop an understanding of operation and maintenance of the electronic system. Students will acquire the ability to identify, analyze, and solve well defined engineering technology problems, with commitment to quality, timeliness, and continuous improvement. The course promotes practicing ethical responsibilities, including respect and diversity.

WEEK	TOPIC	READING ASSIGNMENT	HOMEWORK
1	Introduction to the course. Comparison of digital vs. analog systems.  The binary number system. Digital signals and timing diagram. Parallel vs. serial transmission Binary to decimal conversion Decimal to binary conversion.	Chapter 1 Textbook  pages 4-22	Textbook: Pr. 1.1-1-10
2	Octal number system a) Octal to decimal conversion  b) Octal to binary conversion  c) Binary to octal conversion  Hexadecimal number system. Hex to decimal conversion Hex to binary conversion Hex to octal conversion Binary Coded Decimal BCD Definition of Byte ASCII code Parity (even and odd), Error Detection one bit	Chapter 2 Textbook:  Pages 34-53	Textbook: Pr  2.1-2.6, 2.11, 2.14, 2.20, 2.21, 2.22, and 2.30
3	Logic gates and Boolean algebra AND, OR, INVERTER, gates symbols and truth tables TT Describing the above gates algebraically; Describing logic circuits algebraically; Implementing circuits from a Boolean expression.	Chapter 3 Textbook  Pages 67-83	Textbook: Pr. 3.1, 3.2, 3.11,  3.12, 3.13, 3.16,  and 3.26
4	<b>Exam 1</b>		
5-6	NAND, NOR, and Exclusive OR gates. Booleans Theorems De Morgan's Law Conversion of digital circuits to NAND gates only. Conversion of digital circuits to NOR gates only.	Chapter 3 Textbook Pages 83 – 106	Textbook: Pr. 3.9, 3.22, 3.24, 3.28, 3.29, and  3.38-3.40

WEEK	TOPIC	READING ASSIGNMENT	HOMEWORK
7-8	Sum of products expression Product of sums expression Simplifications of Boolean expressions using Boolean algebra, and Karnaugh maps. Designing combinational logic circuits.	Chapter 4 Textbook: Pages 130-158	Textbook: Pr. 4.1, 4.2, 4.3, 4.5, 4.6, 4.7, 4.22, and 4.23
9	<b>Midterm Examination.</b>		
10	Parity Generator Basic characteristics of IC's (TTL and CMOS) Floating inputs. Trouble shooting digital systems. Exclusive OR gate.	Chapter 4 Textbook: Pages 159-178	4.47
11	Latches and Flip flops NAND gate Latch  Clocked Flip-flops a) S-R Flip-flop b) J-K Flip-flop c) D Flip-flop d) T Flip-flop e) Timing diagrams. Asynchronous inputs f) Input sequence detector circuits	Chapter 5 Textbook: Pages 220 - 254	Textbook: Pr. 5.8, 5.9, 5.11, 5.12, 5.16, 5.17, 5.18, 5.20 – 5.22,
12	Shift registers Counters One Shot device Analyzing sequential circuits	Chapter 5 Textbook: Pages 255-275	Textbook: Pr. 5.27, 5.31, 5.32, and 5.39
13	Binary addition signed numbers 1's complement 2's complement  Addition in the 2's complement system. Subtraction in the 2's complement system. Arithmetic circuits, Full Adder, Full Subtractor.	Chapter 6  Textbook: Pages 310 - 345	Textbook: Pr. 6.1, 6.5, 6.9, 6.10, and 6.18 - 6.20
14	Up-counters Down-counters    Up-down counters Multiplexers	Chapter 7 Textbook: Pages 376 - 413	Textbook: Pr. 7.7 – 7.12
15	<b>Final Examination</b>		