EET1240/ET212 Electronics

Semiconductors and Diodes

Electrical and Telecommunications
Engineering Technology Department

Professor Jang

Prepared by textbook based on "Electronics Devices"
by Floyd, Prentice Hall, 7th edition.

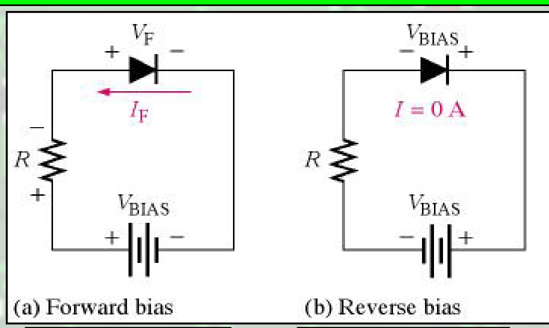
Outline

- Semiconductor Physics
- The PN junction
- Biasing the PN junction
- The diode
- Trouble Shooting

Key Words: Semiconductor, Silicon, PN Junction, Forward Bias, Reverse Bias, Diode

Introduction

The basic function of a diode is to restrict current flow to one direction.



Forward bias
Current flows

Reverse Bias
No current flow

Bohr model of an atom

As seen in this model, electrons circle the nucleus. Atomic structure of a material determines it's ability to conduct or insulate.

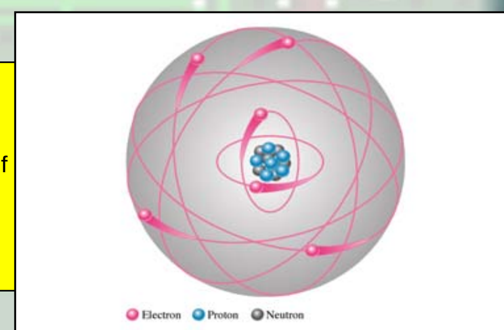


FIGURE 1 The Bohr model of an atom showing electrons in orbits and around the nucleus, which consists of protons and neutrons. The "tails" on the electrons indicate motion.

The two simplest atoms

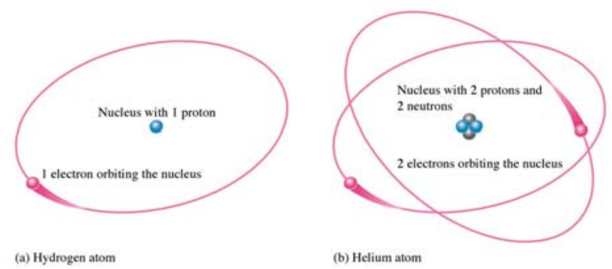


FIGURE 2 The two simplest atoms, hydrogen and helium.

Conductors, Insulators, and Semiconductors

- The ability of a material to conduct current is based on its atomic structure.
- The orbit paths of the electrons surrounding the nucleus are called shells.
- Each shell has a defined number of electrons it will hold. This is a fact of nature and can be determined by the formula, $N_e = 2n^2$.
- The outer shell is called the valence shell.
- The less complete a shell is filled to capacity the more conductive the material is.

Atomic number, Electron shells & Orbits, Valence electrons, and Ionization

- All elements are arranged in the periodic table of the elements in order according to their atomic number.

  The atomic number equals the number of protons in the nucleus, which is the same as the number electrons.
- Electron shells and Orbits
- The outmost shell is known as the Valence shell and electrons in this shell are called valence electrons.
- The process of losing a valence electron is known as ionization (i.e. *positive ion* and *negative ion*).

Electron shells and Orbits

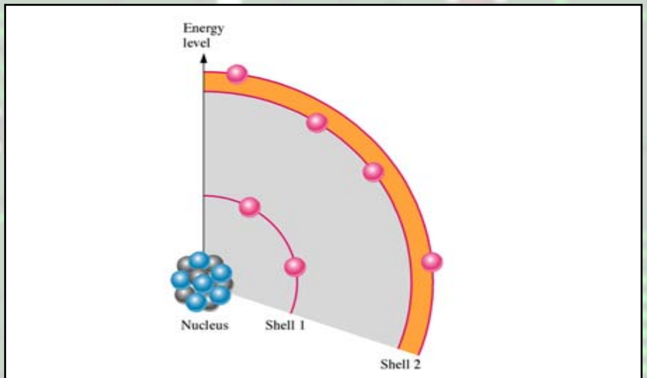


FIGURE 3 Energy levels increase as the distance from the nucleus increases.

Conductors, Insulators, and Semiconductors

- A **conductor** is a material that easily conducts electrical current. The best conductors are single-element material, such as copper, gold, and aluminum, which are characterized by atoms with only one valence electron very loosely bound to the atom.
- An **insulator** is a material that does not conduct electrical current under normal conditions. Valence electrons are tightly bound to the atoms.
- A **semiconductor** is a material that is between conductors and insulators in its ability to conduct electrical current. The most common single –element semiconductors are silicon, germanium, and carbon.

Energy Bands

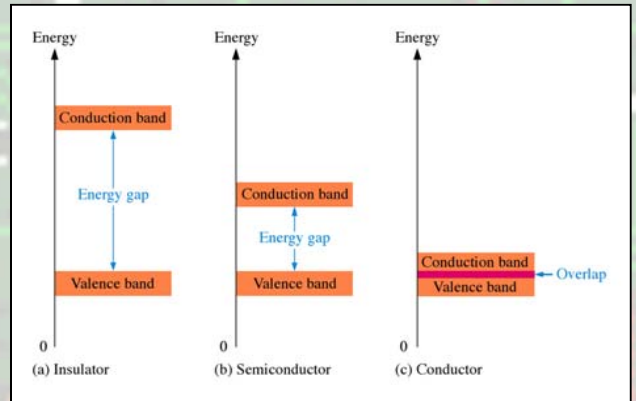


FIGURE 4 Energy band diagram for a pure (intrinsic) silicon crystal with unexcited atoms. There are no electrons in the conduction band.

Conductors, Insulators, and Semiconductors

The valence shell determines the ability of material to conduct current.

A Silicon atom has 4 electrons in its valence ring. This makes it a semiconductor. It takes $2n^2$ electrons or in this case or 18 electrons to fill the valence shell.

A Copper atom has only 1 electron in it's valence ring. This makes it a good conductor. It takes $2n^2$ electrons or in this case 32 electrons to fill the valence shell.

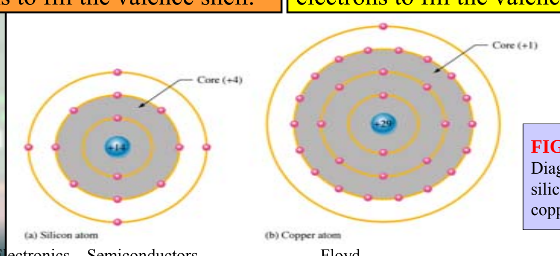
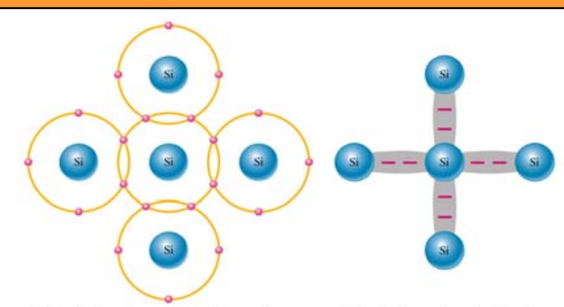


FIGURE 5 Diagrams of the silicon and copper atoms.

Covalent Bonding

Covalent bonding is a bonding of two or more atoms by the interaction of their valence electrons.



(a) The center atom shares an electron with each of the four surrounding atoms, creating a covalent bond with each. The surrounding atoms are in turn bonded to other atoms, and so on.

(b) Bonding diagram. The red negative signs represent the shared valence electrons.

FIGURE 6

Silicon and Germanium

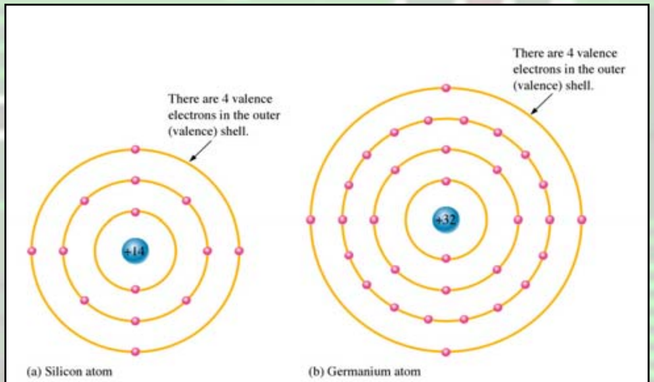


FIGURE 7 Diagrams of the silicon and germanium atoms.

Conduction in Semiconductors

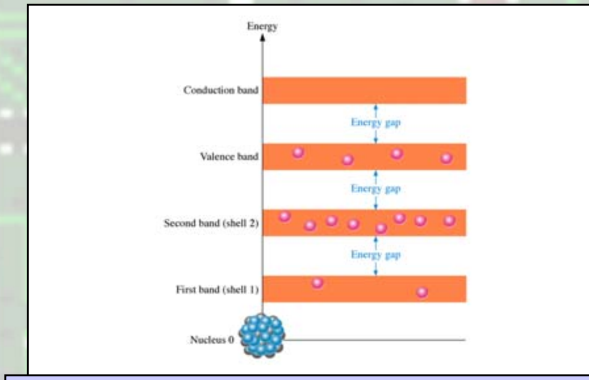


FIGURE 9 Energy band diagram for a pure (intrinsic) silicon crystal with unexcited atoms. There are no electrons in the conduction band.

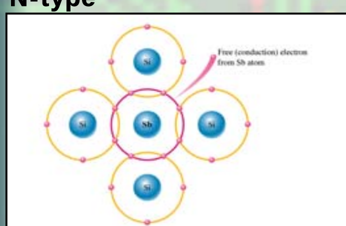
N-type and P-type Semiconductors

The process of creating N and P type materials is called doping.

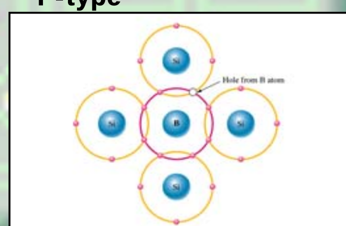
Other atoms with 5 electrons (pentavalent atom) such as Antimony are added to Silicon to increase the free electrons.

Other atoms with 3 electrons (trivalent atoms) such as Boron are added to Silicon to create a deficiency of electrons or hole charges.

N-type

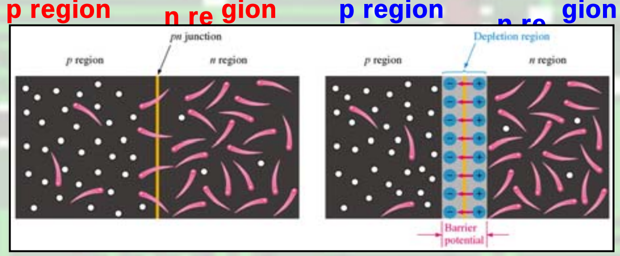


P-type



The Depletion Region

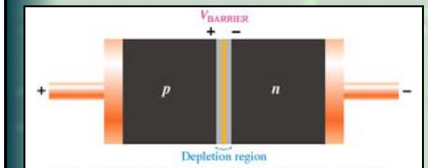
p region n re gion p region gion



With the formation of the p and n materials combination of electrons and holes at the junction takes place.

This creates the depletion region and has a barrier potential. This potential cannot be measured with a voltmeter but it will cause a small voltage drop.

Biasing the Diode : Forward and Reverse Bias

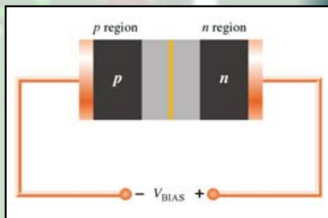


(b) Forward bias narrows the depletion region and produces a voltage drop across the *pn* junction equal to the barrier potential.

Voltage source or bias connections are + to the p material and – to the n material

Bias must be greater than .3 V for Germanium or .7 V for Silicon diodes.

The depletion region narrows.



Voltage source or bias connections are – to the p material and + to the n material.

Bias must be less than the break down voltage.

Current flow is negligible in most cases.

The depletion region widens.

Forward Bias

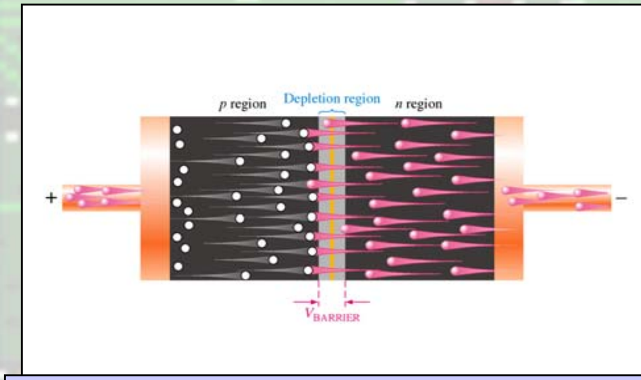


FIGURE 10 A forward-biased diode showing the flow of majority carriers and the voltage due to the barrier potential across the depletion region.

Reverse Bias

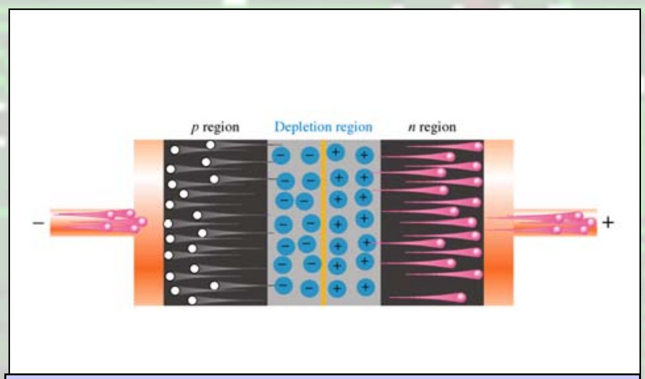
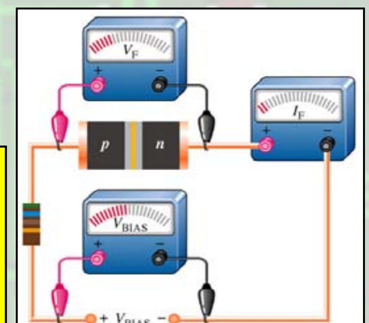


FIGURE 11 The diode during the short transition time immediately after reverse-bias voltage is applied.

Forward Bias Measurements With Small Voltage Applied

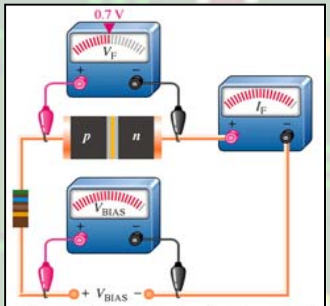
In this case with the voltage applied is less than the barrier potential so the diode for all practical purposes is still in a non-conducting state. Current is very small.



(a) Small forward-bias voltage ($V_F < 0.7$ V), very small forward current.

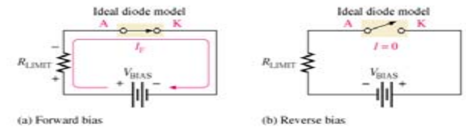
Forward Bias Measurements With Applied Voltage Greater Than the Barrier Voltage.

With the applied voltage exceeding the barrier potential the now fully forward biased diode conducts. Note that the only practical loss is the .7 Volts dropped across the diode.

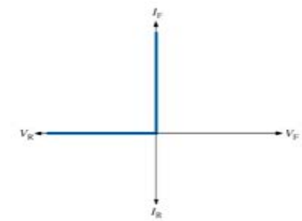


(b) Forward voltage reaches and remains at approximately 0.7 V. Forward current continues to increase as the bias voltage is increased.

Ideal Diode Characteristic Curve

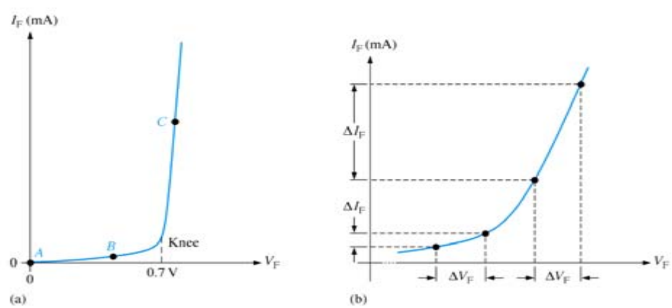


In this characteristic curve we do not consider the voltage drop or the resistive properties. Current flow proportionally increases with voltage.



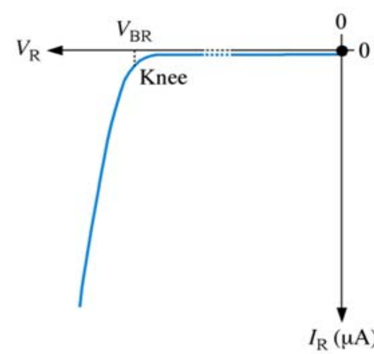
(c) Ideal characteristic curve (blue)

V-I Characteristic for Forward Bias



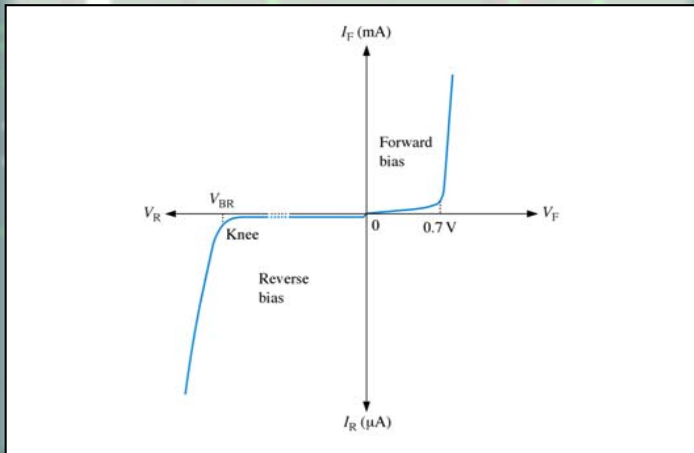
(a) V-I characteristic curve for forward bias. Part (b) illustrates how the dynamic resistance r'_d decreases as you move up the curve ($r'_d = \Delta V_F/\Delta I_F$).

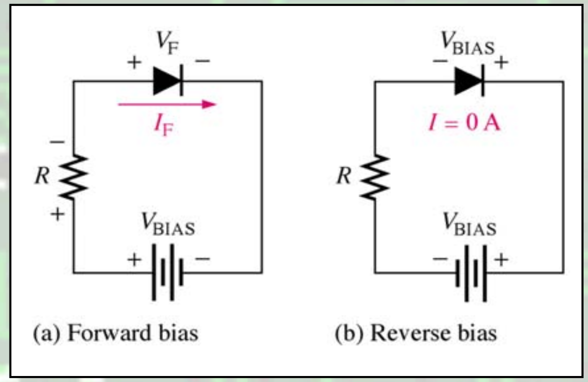
V-I Characteristic for Reverse Bias



V-I characteristic curve for reverse-biased diode.

The complete V-I characteristic curve for a diode

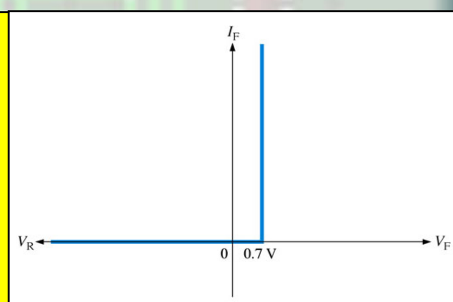




Forward-bias and reverse-bias connections showing the diode symbol.

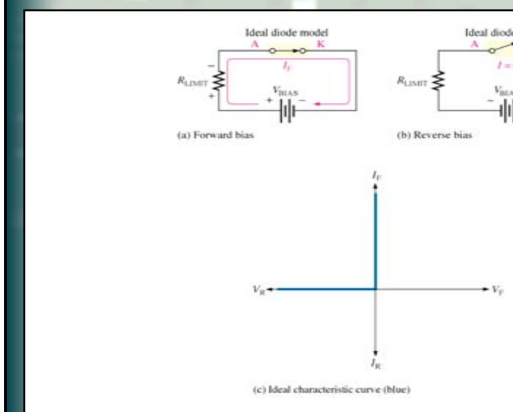
Practical Diode Characteristic Curve

In most cases we consider only the forward bias voltage drop of a diode. Once this voltage is overcome the current increases proportionally with voltage.This drop is particularly important to consider in low voltage applications.



(c) Characteristic curve (silicon)

The Ideal Diode Model



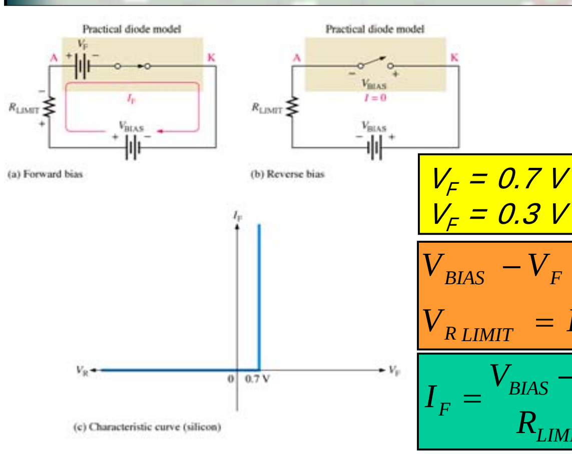
$V_F = 0\ V$

$$I_F = \frac{V_{BIAS}}{R_{LIMIT}}$$

$I_R = 0\ A$

$V_R = V_{BIAS}$

The Practical Diode Model



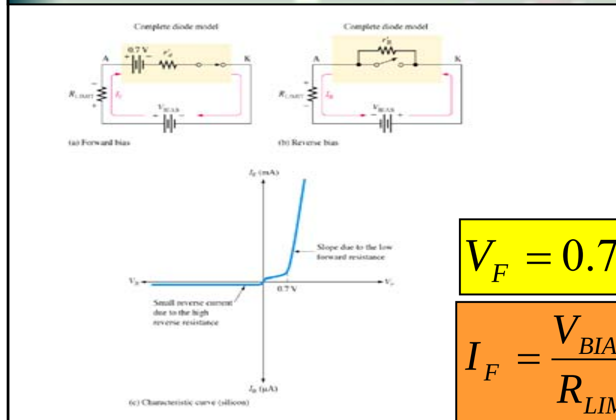
V_F = 0.7 V (silicon)
V_F = 0.3 V (germanium)

$$V_{BIAS} - V_F - V_{R_{LIMIT}} = 0$$

$$V_{R\,LIMIT} = I_F R_{LIMIT}$$

$$I_F = \frac{V_{BIAS} - V_F}{R_{LIMIT}}$$

The Complete Diode Model



$$V_F = 0.7 + I_F r_d'$$

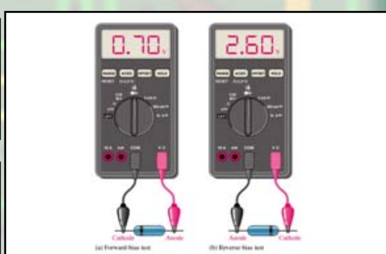
$$I_F = \frac{V_{BIAS} - 0.7}{R_{LIMIT} + r_d'}$$

Troubleshooting Diodes

Testing a diode is quite simple, particularly if the multimeter used has a diode check function. With the diode check function a specific known voltage is applied from the meter across the diode.

With the diode check function a good diode will show approximately .7 V or .3 V when forward biased.

When checking in reverse bias the full applied testing voltage will be seen on the display.



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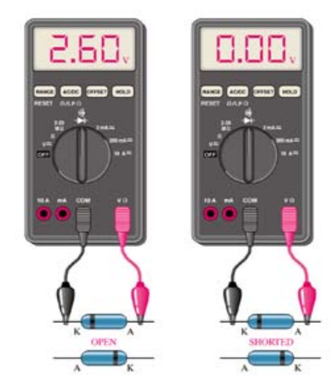
Troubleshooting Diodes

Open Diode

In the case of an *open diode* no current flows in either direction which is indicated by the full checking voltage with the diode check function or high resistance using an ohmmeter in both forward and reverse connections.

Shorted Diode

In the case of a *shorted diode* maximum current flows indicated by a 0 V with the diode check function or low resistance with an ohmmeter in both forward and reverse connections.



(a) Forward- and reverse-bias tests for an open diode give same indication. Some meters will display "OL."

(b) Forward- and reverse-bias tests for a shorted diode give same 0 V reading. If the diode is resistive, the reading is less than 2.6 V.

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Diode Applications

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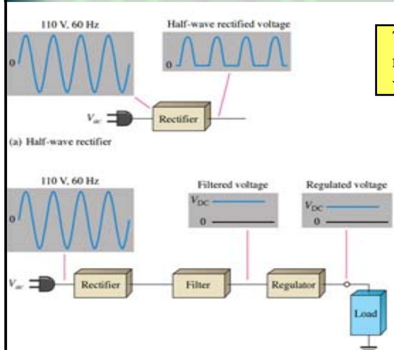
Outlines

- Half Wave Rectifiers
- Full Wave Rectifier
- DC Power Supply Filter and Regulator
- IC Regulator
- Zener Diode
- Troubleshoot

Key Words: Half Wave, Full Wave, Rectifier, Power Supply, Regulator, Zener

Introduction

The basic function of a DC power supply is to convert an AC voltage (110 V, 60 Hz) to a smooth DC voltage.



(a) Half-wave rectifier
(b) Complete power supply with rectifier, filter, and regulator

The **rectifier** can be either a half- or Full-wave rectifier. The rectifier convert the ac input voltage to a pulsating dc voltage.

The **filter** eliminates the fluctuation in the rectified voltage and produces a relatively smooth dc voltage.

The **regulator** is a circuit that maintains a constant dc voltage for variations in the input power line voltage or in the load.

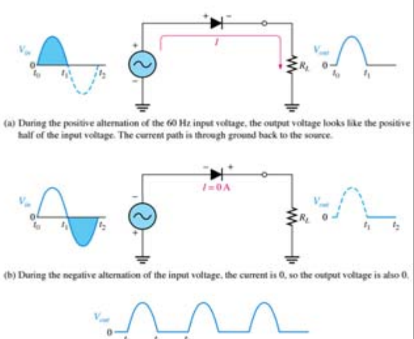
Half Wave Rectifier

A half wave rectifier(ideal) allows conduction for only 180° or half of a complete cycle. The output frequency is the same as the input. The average V_{DC} or $V_{AVG} = V_p/\pi$

When the sinusoidal input voltage (V_{in}) goes positive, the diode is forward-biased and conducts current through the load resistor. The current produces an output voltage across the load R_L.

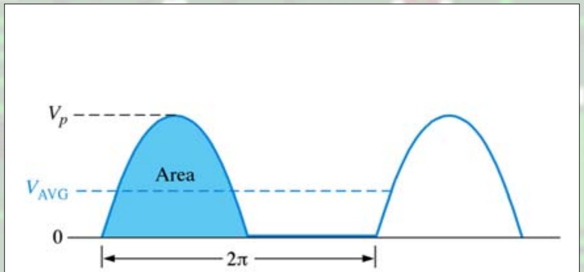
When the input voltage goes negative during the second half of its cycle, the diode reversed-biased. There is no current, so the voltage across the load resistor is 0 V.

The net result is that only the positive half-cycles of the ac input voltage appear across the load. Since the output does not change polarity, it is pulsating dc voltage with a frequency of 60 Hz.



(a) During the positive alternation of the 60 Hz input voltage, the output voltage looks like the positive half of the input voltage. The current path is through ground back to the source.
(b) During the negative alternation of the input voltage, the current is 0, so the output voltage is also 0.
(c) 60 Hz half-wave output voltage for three input cycles

Average value of the half-wave rectified signal



$$v = V_p \sin \theta$$

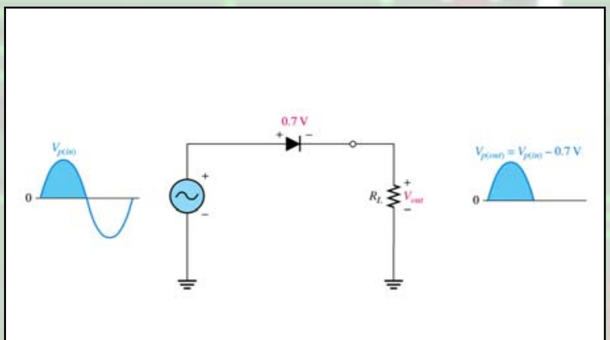
$$V_{AVG} = \frac{area}{2\pi} = \frac{1}{2\pi}\int_0^{\pi} V_p \sin\theta \, d\theta = \frac{V_p}{2\pi}[-\cos\pi - (-\cos 0)]$$

$$= \frac{V_p}{2\pi}[-(-1) - (-1)] = \frac{V_p}{2\pi}(2) = \frac{V_p}{\pi}$$

Ex 2-1 **What is the average value of the half-wave rectified voltage in Figure?**

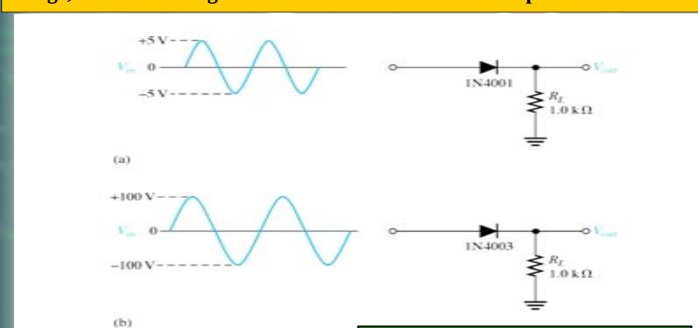
$$V_{AVG} = \frac{V_p}{\pi} = \frac{100}{\pi} = 31.8V$$

Effect of the Barrier Potential on the Half-Wave Rectified Output



The effect of the barrier potential on the half-wave rectified output voltage is to reduce the peak value of the input by about 0.7 V.

Ex 2-2 **Sketch the output voltages of each rectifier for the indicated input voltage, as shown in Figure. The IN4001 and IN4003 are specific rectifier diodes.**



The peak output voltage for circuit (a) is

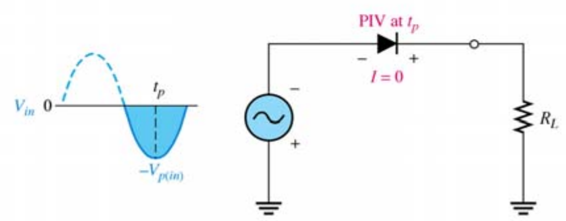
$V_{p(out)} = V_{p(in)} - 0.7$ V
$= 5$ V $- 0.7$ V $= 4.30$ V

The peak output voltage for circuit (b) is

$V_{p(out)} = V_{p(in)} - 0.7$ V
$= 100$ V $- 0.7$ V $= 99.30$ V

Half Wave Rectifier - Peak Inverse Voltage (PIV)

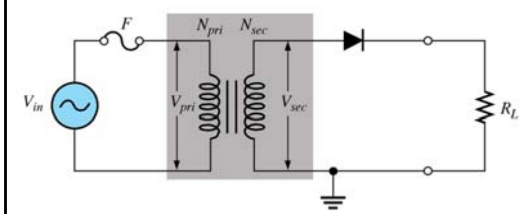
Peak inverse voltage is the maximum voltage across the diode when it is in reverse bias. The diode must be capable of withstanding this amount of voltage. PIV = $V_{p(in)}$



The PIV occurs at the peak of each half-cycle of the input voltage when the diode is reverse-biased. In this circuit, the PIV occurs at the peak of each negative half-cycle.

Half Wave Rectifier with Transformer-Coupled Input Voltage

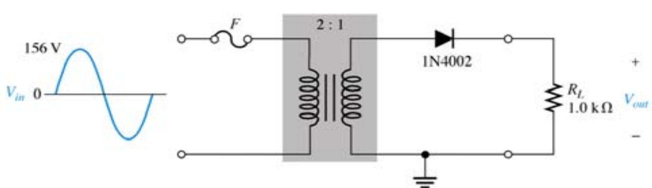
Transformer coupling provides two advantages. First, it allows the source voltage to be stepped up or stepped down as needed. Second, the ac source is electrically isolated from the rectifier, thus preventing a shock hazard in the secondary circuit.



$V_{sec} = nV_{pri}$
where $n = N_{sec}/N_{pri}$
If n>1, stepped up transformer
If n<1, Stepped down transformer
$V_{p(out)} = V_{p(sec)} – 0.7$ V

Figure Half-wave rectifier with transformer-coupled input voltage.

Ex 2-3 Determine the peak value of the output voltage for Figure if the turns ratio is 0.5.

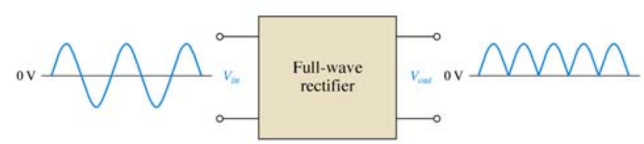


$V_{p(pri)} = V_{p(in)} = 156$ V
The peak secondary voltage is
$V_{p(sec)} = nV_{p(pri)} = 78$ V
The rectified peak output voltage is
$V_{p(out)} = V_{p(sec)} – 0.7$ V
$= 78$ V – 0.7 V = 77.3 V

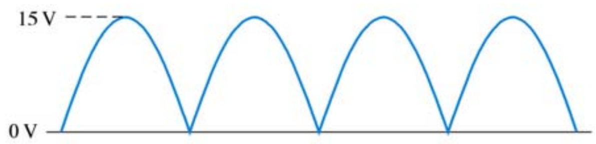
Full-Wave Rectifiers

A full-wave rectifier allows current to flow during both the positive and negative half cycles or the **full 360°**. Note that the output frequency is twice the input frequency.

$$V_{AVG} = \frac{2V_p}{\pi}$$



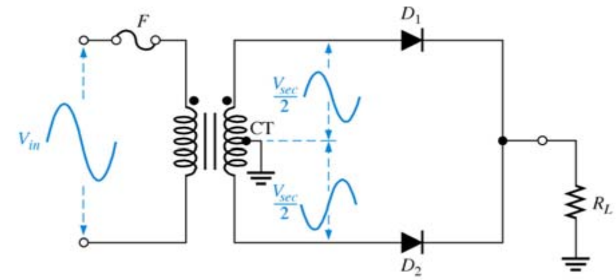
Ex 2-4 **Find the average value of the full-wave rectified voltage in Figure.**



$$V_{AVG} = \frac{2V_p}{\pi} = \frac{2(15)}{\pi} = 9.55\,V$$

The Center-Tapped Full-Wave Rectifier

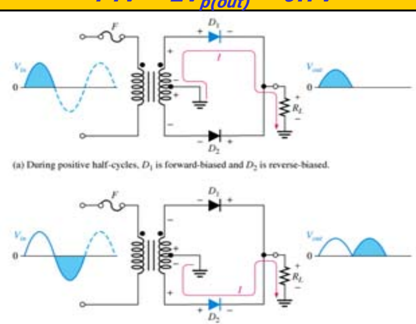
This method of rectification employs two diodes connected to a center-tapped transformer. The peak output is only half of the transformer's peak secondary voltage.



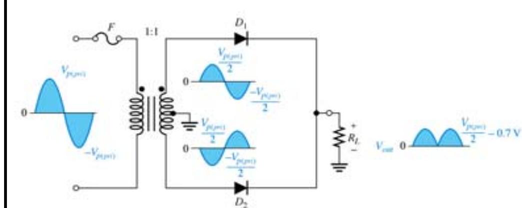
Full-Wave Center Tapped

Note the current flow direction during both alternations. Being that it is center tapped, the peak output is about half of the secondary windings total voltage. Each diode is subjected to a PIV of the full secondary winding output minus one diode voltage drop

$$PIV = 2V_{p(out)} + 0.7V$$

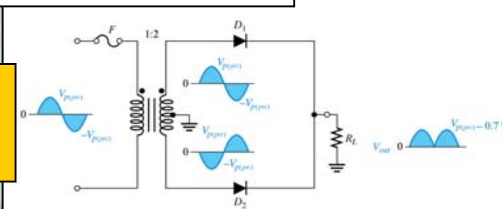


(a) During positive half-cycles, D_1 is forward-biased and D_2 is reverse-biased.

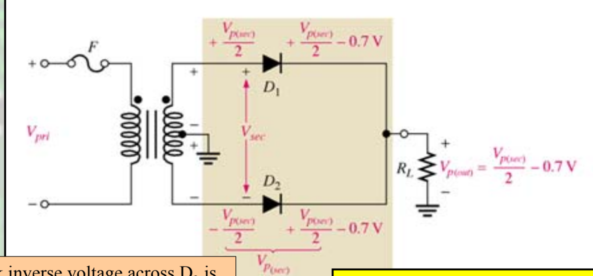


Center-tapped full-wave rectifier with a transformer turns ratio of 1. $V_{p(pri)}$ is the peak value of the primary voltage.

Center-tapped full-wave rectifier with a transformer turns ratio of 2.



Full Wave Rectifier - Peak Inverse Voltage (PIV)



The peak inverse voltage across D_2 is

$$PIV = \left(\frac{V_{p(sec)}}{2} - 0.7\right) - \left(\frac{-V_{p(sec)}}{2}\right)$$

$$= \frac{V_{p(sec)}}{2} + \frac{V_{p(sec)}}{2} - 0.7V$$

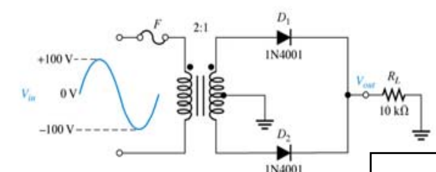
$$= V_{p(sec)} - 0.7V$$

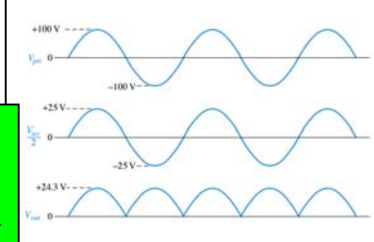
$V_{p(out)} = V_{p(sec)}/2 - 0.7$ V

$V_{p(sec)} = 2V_{p(out)} + 1.4$ V

PIV = $2V_{p(out)} + 0.7$ V

Ex 2-5 Show the voltage waveforms across each half of the secondary winding and across R_L when a 100 V peak sine wave is applied to the primary winding in Figure. Also, what minimum PIV rating must the diodes have?

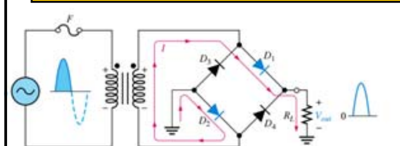




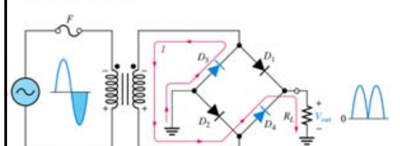
$V_{p(sec)} = nV_{p(pri)} = 0.5(100\text{ V}) = 50$ V
There is a 25 V peak across each half of the secondary with respect to ground. The output load voltage has a peak value of 25 V, less the 0.7 V drop across the diode.
PIV = $V_{p(sec)} - 0.7$ V = 50 V – 0.7 V = 49.3 V

The Full-Wave Bridge Rectifier

The full-wave bridge rectifier takes advantage of the full output of the secondary winding. It employs four diodes arranged such that current flows in the direction through the load during each half of the cycle.



During positive half-cycle of the input, D_1 and D_2 are forward-biased and conduct current. D_3 and D_4 are reverse-biased.

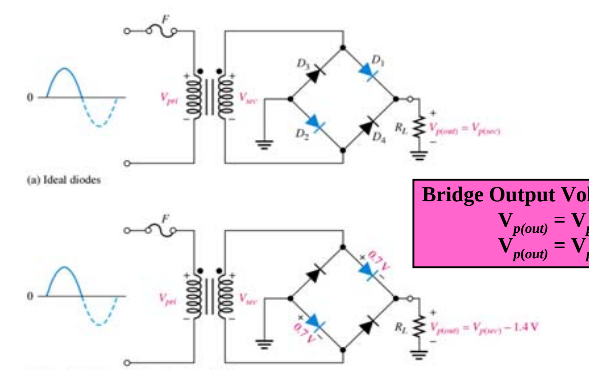


During negative half-cycle of the input, D_3 and D_4 are forward-biased and conduct current. D_1 and D_2 are reverse-biased.

When the input cycle is positive as in part (a), diode D_1 and D_2 are forward-biased and conduct current in the direction shown. A voltage is developed across R_L which looks like the positive half of the input cycle. During this time, diodes D_3 and D_4 are reverse-biased.

When the input cycle is negative as in part (b), diode D_3 and D_4 are forward-biased and conduct current in the same direction through R_L as during the positive half-cycle. During negative half-cycle, D_1 and D_2 are reverse-biased. A full-wave rectified output voltage appears across R_L as a result of this action.

The Full-Wave Bridge Rectifier-Peak Inverse Voltage



(a) Ideal diodes

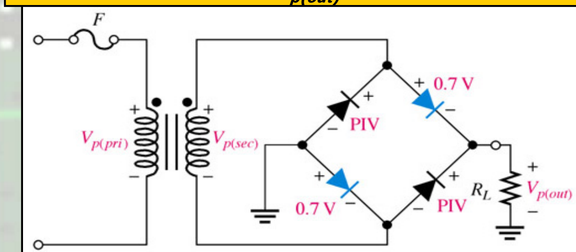
(b) Practical diodes (Diode drops included)

Bridge Output Voltage:
$V_{p(out)} = V_{p(sec)}$
$V_{p(out)} = V_{p(sec)} - 1.4$ V

The Full-Wave Bridge Rectifier

The PIV for a bridge rectifier is approximately half the PIV for a center-tapped rectifier.

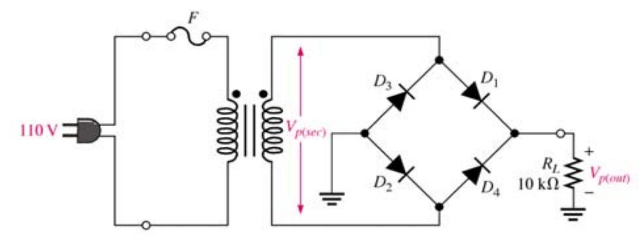
$$PIV = V_{p(out)} + 0.7V$$



(b) For the practical diode model (forward-biased diodes D_1 and D_2 are shown in blue). PIV = $V_{p(out)}$ + 0.7 V

Note that in most cases we take the diode drop into account.

Ex 2-6 Determine the peak output voltage for the bridge rectifier in Figure. Assuming the practical model, what PIV rating is required for the diodes? The transformer is specified to have a 12 V_{rms} secondary voltage for the standard 110 V across the primary.



$V_{p(sec)} = 1.414V_{rms} = 1.414(12\text{ V}) \approx 17\text{ V}$

$V_{p(out)} = V_{p(sec)} - 1.4\text{ V} = 17\text{ V} - 1.4\text{ V} = 15.6\text{ V}$

$PIV = V_{p(out)} + 0.7\text{ V} = 15.6\text{ V} + 0.7\text{ V} = 16.3\text{ V}$

Power Supply Filters And Regulators

As we have seen, the output of a rectifier is a pulsating DC. With filtration and regulation this pulsating voltage can be smoothed out and kept to a **steady value**.

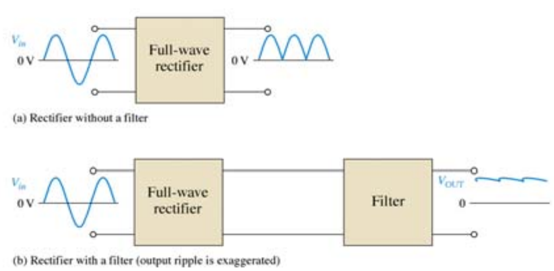
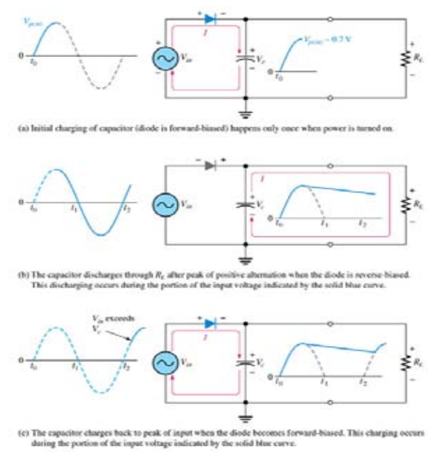


Figure illustrates the filtering concept showing a nearly smooth dc output voltage from filter. The small amount of fluctuation in the filter output voltage is called ripple.

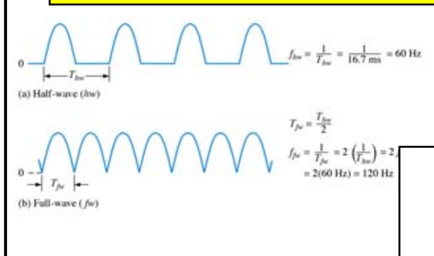
Power Supply Filters and Regulators

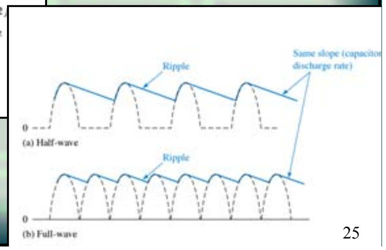
A capacitor-input filter will charge and discharge such that it fills in the "gaps" between each peak. This reduces variations of voltage. This voltage variation is called ripple voltage.



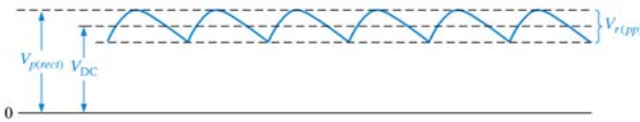
Power Supply Filters And Regulators

The advantage of a full-wave rectifier over a half-wave is quite clear. The capacitor can more effectively reduce the ripple when the time between peaks is shorter.





Ripple Factor



The **ripple factor *(r)*** is an indication of the effectiveness of the filter and defined as

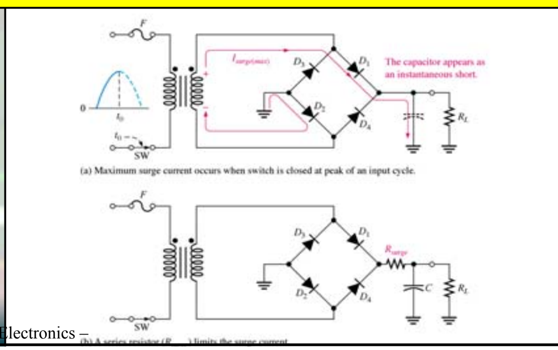
$$r = V_{r(pp)} / V_{DC}$$

$$V_{r(pp)} \cong \left(\frac{1}{fR_LC}\right)V_{p(rect)}$$

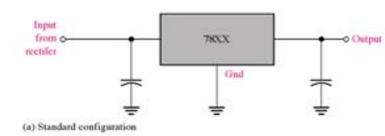
$$V_{DC} \cong \left(1 - \frac{1}{2fR_LC}\right)V_{p(rect)}$$

Surge Current in the Capacitor-Input Filter

Being that the capacitor appears as a short during the initial charging, the current through the diodes can momentarily be quite high. To reduce risk of damaging the diodes, a surge current limiting resistor is placed in series with the filter and load.

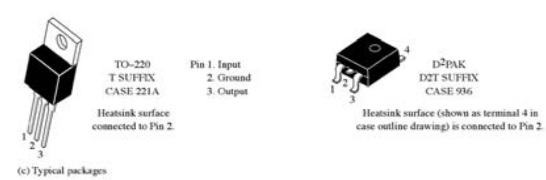


IC Regulators



Type number	Output voltage
7805	+5.0 V
7806	+6.0 V
7808	+8.0 V
7809	+9.0 V
7812	+12.0 V
7815	+15.0 V
7818	+18.0 V
7824	+24.0 V

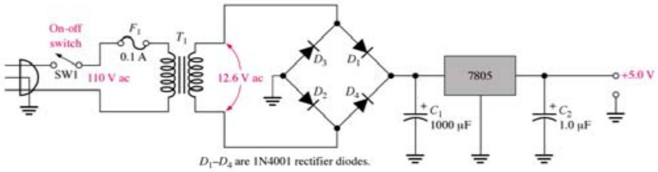
(b) The 7800 series



The 7800 series three-terminal fixed positive voltage regulators.

Power Supply Filters And Regulators

Regulation is the last step in eliminating the remaining ripple and maintaining the output voltage to a specific value. Typically this regulation is performed by an integrated circuit regulator. There are many different types used based on the voltage and current requirements.



Power Supply Filters and Regulators

How well the regulation is performed by a regulator is measured by its regulation percentage. There are two types of regulation, line and load. Line and load regulation percentage is simply a ratio of change in voltage (line) or current (load) stated as a percentage.

Line Regulation = $(\Delta V_{OUT}/\Delta V_{IN})100\%$

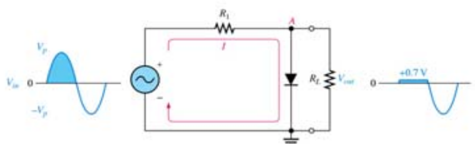
Load Regulation = $((V_{NL} - V_{FL})/ V_{FL})100\%$

Load Regulation =

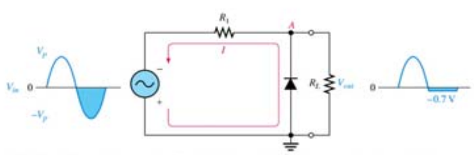
$$(\frac{V_{NL} - V_{FL}}{V_{FL}})100\% = (\frac{5.185V - 5.152V}{5.152V})100\% = 0.64\%$$

Diode Limiters

Limiting circuits limit the positive or negative amount of an input voltage to a specific value.



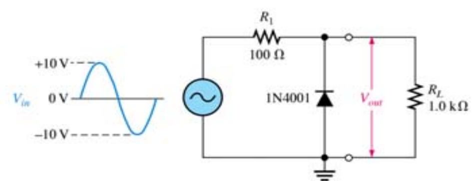
(a) Limiting of the positive alternation. The diode is forward-biased during the positive alternation (above 0.7 V) and reverse-biased during the negative alternation.



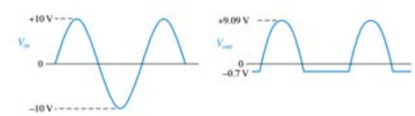
(b) Limiting of the negative alternation. The diode is forward-biased during the negative alternation (below −0.7 V) and reverse-biased during the positive alternation.

$$V_{out} = (\frac{R_L}{R_1 + R_L})V_{in}$$

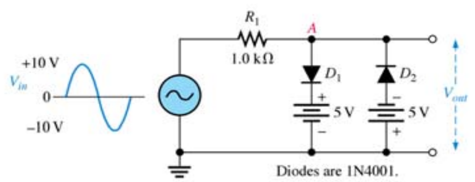
Ex 2-7 What would you expect to see displayed on an oscilloscope connected across R_L in the limiter shown in Figure.

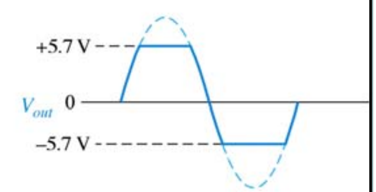


$$V_{p(out)} = (\frac{R_L}{R_1 + R_L})V_{p(in)} = (\frac{1.0k\Omega}{1.1k\Omega})10V = 9.09V$$

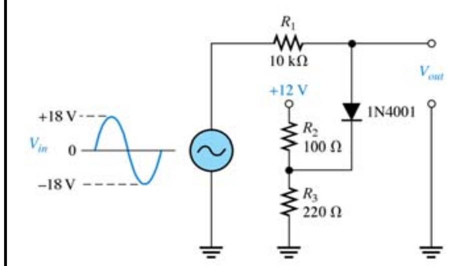


Ex 2-8 **Figure shows a circuit combining a positive limiter. Determine the output voltage waveform.**





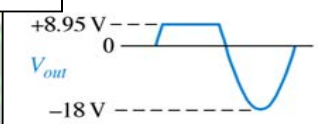
Ex 2-9 **Describe the output voltage waveform for the diode limiter in Figure.**



$$V_{BIAS} = \left(\frac{R_3}{R_2 + R_3}\right)V_{SUPPLY}$$

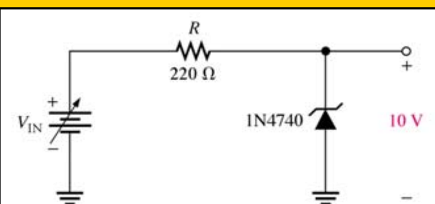
$$= \left(\frac{220\Omega}{100\Omega + 220\Omega}\right)12V$$

$$= 8.25V$$



Introduction – Zener Diode

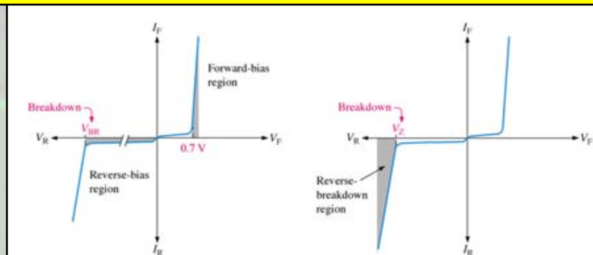
The **zener diode** is a silicon pn junction devices that differs from rectifier diodes because *it is designed for operation in the reverse-breakdown region*. The breakdown voltage of a zener diode is set by carefully controlling the level during manufacture. The basic function of **zener diode** is to maintain a specific voltage across its terminals within given limits of line or load change. Typically it is used for providing a stable reference voltage for use in power supplies and other equipment.



This particular zener circuit will work to maintain 10 V across the load.

Zener Diodes

A **zener diode** is much like a normal diode. The exception being is that it is placed in the circuit in reverse bias and operates in reverse breakdown. This typical characteristic curve illustrates the operating range for a zener. Note that its forward characteristics are just like a normal diode.



(a) The normal operating regions for a rectifier diode are shown as shaded areas.

(b) The normal operating region for a zener diode is shaded.

Volt-ampere characteristic is shown in this Figure with normal operating regions for rectifier diodes and for zener diodes shown as shaded areas.

Zener Breakdown

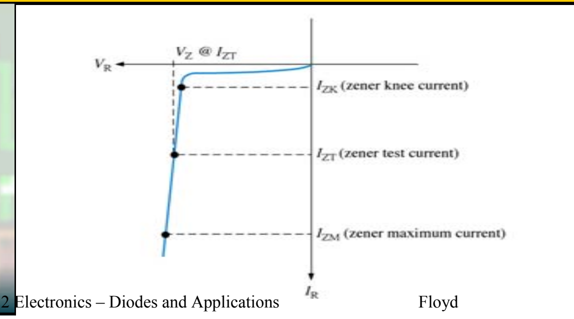
Zener diodes are designed to operate in reverse breakdown. Two types of reverse breakdown in a zener diode are *avalanche* and *zener*. The avalanche break down occurs in both rectifier and zener diodes at a sufficiently high reverse voltage. Zener breakdown occurs in a zener diode at low reverse voltages.

A zener diode is heavily doped to reduced the breakdown voltage. This causes a very thin depletion region. As a result, an intense electric field exists within the depletion region. Near the zener breakdown voltage (V_z), the field is intense enough to pull electrons from their valence bands and create current. The zener diodes breakdown characteristics are determined by the doping process

Low voltage zeners less than 5V operate in the zener breakdown range. Those designed to operate more than 5 V operate mostly in **avalanche breakdown** range. Zeners are commercially available with voltage breakdowns of 1.8 V to 200 V.

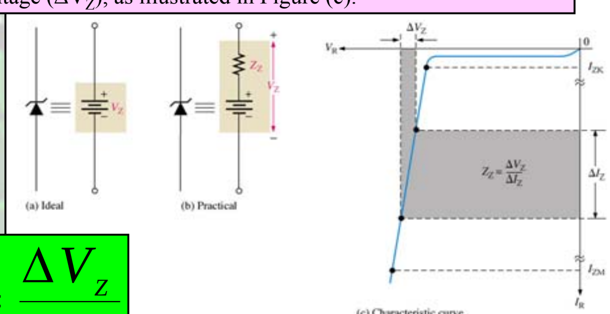
Breakdown Characteristics

Figure shows the reverse portion of a zener diode's characteristic curve. As the reverse voltage (V_R) is increased, the reverse current (I_R) remains extremely small up to the "knee" of the curve. The reverse current is also called the zener current, I_Z. At this point, the breakdown effect begins; the internal zener resistance, also called zener impedance (Z_Z), begins to decrease as reverse current increases rapidly.



Zener Equivalent Circuit

Figure (b) represents the practical model of a zener diode, where the zener impedance (Z_Z) is included. Since the actual voltage curve is not ideally vertical, a change in zener current (ΔI_Z) produces a small change in zener voltage (ΔV_Z), as illustrated in Figure (c).

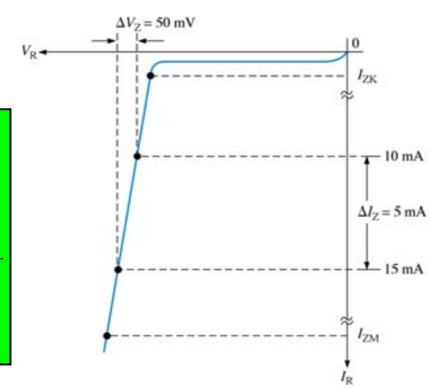


$$Z_Z = \frac{\Delta V_Z}{\Delta I_Z}$$

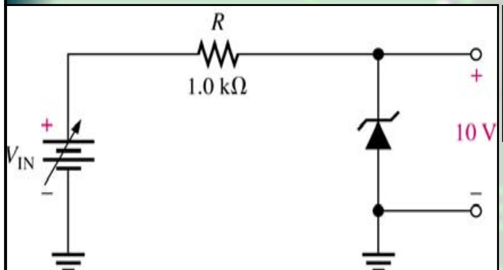
Zener diode equivalent circuit models and the characteristic curve illustrating Z_Z.

Ex 2-10 A zener diode exhibits a certain change in V_Z for a certain change in I_Z on a portion of the linear characteristic curve between I_{ZK} and I_{ZM} as illustrated in Figure. What is the zener impedance?

$$Z_Z = \frac{\Delta V_Z}{\Delta I_Z} = \frac{50\,mV}{5\,mV} = 10\,\Omega$$



Ex 2-11 Figure shows a zener diode regulator designed to hold 10 V at the output. Assume the zener current ranges from 4 mA maximum (I_{ZK}) to 40 mA maximum (I_{ZM}). What are the minimum and maximum input voltages for these current?.



For minimum current, The voltage across the 1.0 kΩ resistor is

$V_R = I_{ZK} \cdot R$
$= (4\text{ mA})(1\text{ k}\Omega) = 4\text{ V}$

Since $V_R = V_{IN} - V_Z$,
$V_{IN} = V_R + V_Z$
$= 4\text{ V} + 10\text{ V} = 14\text{ V}$

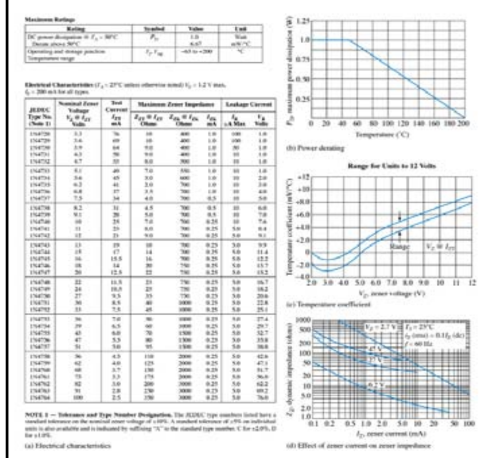
For the maximum zener current, the voltage across the 1.0 kΩ resistor is

$V_R = (40\text{ mA})(1.0\text{ k}\Omega) = 40\text{ V}$

Therefore,

$V_{IN} = 40\text{ V} + 10\text{ V} = 50\text{ V}$

Zener diode Data Sheet Information

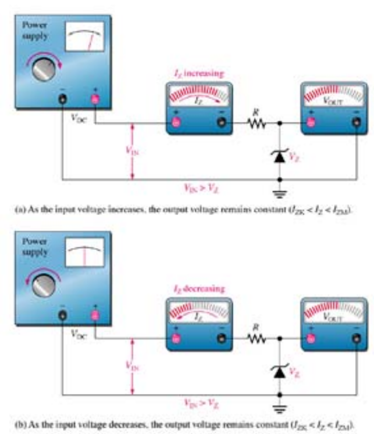


Partial data sheet for the 1N4728-1N4764 series 1 W zener diodes.

As with most devices, zener diodes have given characteristics such as temperature coefficients and power ratings that have to be considered. The data sheet provides this information.

- V_Z: zener voltage
- I_{ZT}: zener test current
- Z_{ZT}: zener Impedance
- I_{ZK}: zener knee current
- I_{ZM}: maximum zener current

Zener Diode Applications – Zener Regulation with a Varying Input Voltage

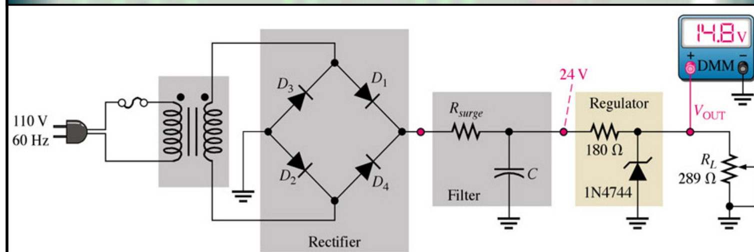


(a) As the input voltage increases, the output voltage remains constant ($I_{ZK} < I_Z < I_{ZM}$).

(b) As the input voltage decreases, the output voltage remains constant ($I_{ZK} < I_Z < I_{ZM}$).

Troubleshooting

Although precise power supplies typically use IC type regulators, zener diodes can be used alone as a voltage regulator. As with all troubleshooting techniques we must know what is normal.



(b) Correct output voltage with full load

A properly functioning zener will work to maintain the output voltage within certain limits despite changes in load.

EET1240/ET212 Electronics

Special Purpose Diodes

Electrical and Telecommunications Engineering Technology Department

Professor Jang

Prepared by textbook based on "Electronics Devices" by Floyd, Prentice Hall, 7th edition.

Outlines

- **Introduction to Zener Diode**
- **Voltage regulation and limiting**
- **The varactor diode**
- **LEDs and photodiodes**
- **Special Diodes**

Key Words: Zener Diode, Voltage Regulation, LED, Photodiode, Special Diode

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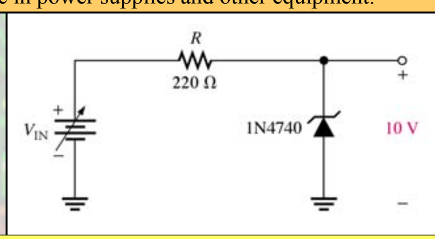

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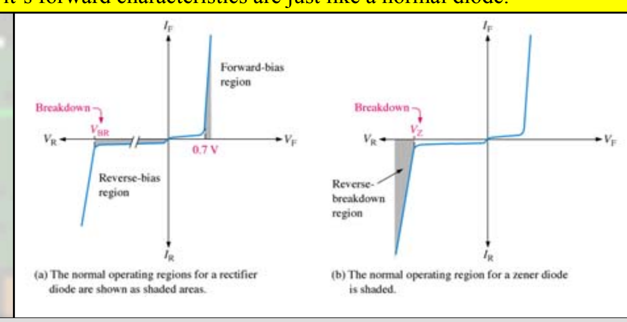

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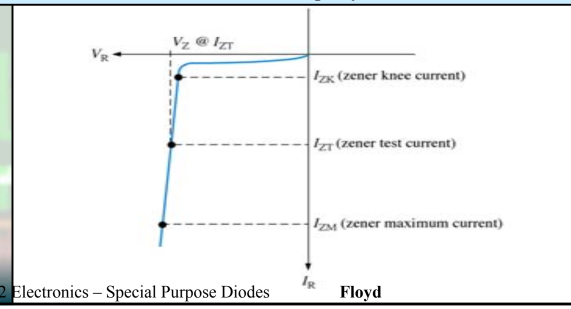
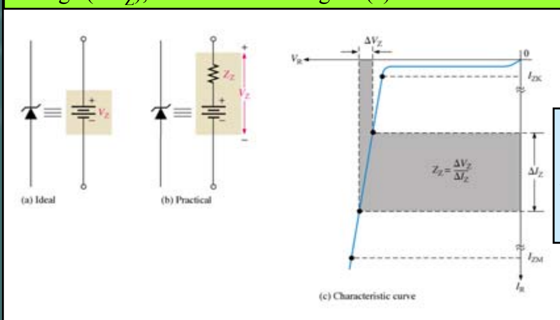
Breakdown Characteristics

Figure shows the reverse portion of a zener diode's characteristic curve. As the reverse voltage (V_R) is increased, the reverse current (I_R) remains extremely small up to the "knee" of the curve. The reverse current is also called the zener current, I_Z. At this point, the breakdown effect begins; the internal zener resistance, also called zener impedance (Z_Z), begins to decrease as reverse current increases rapidly.



Zener Equivalent Circuit

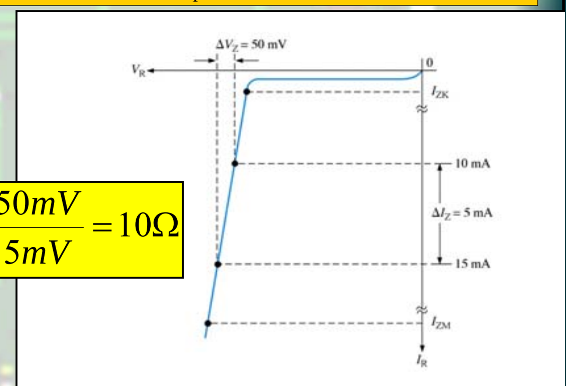
Figure (b) represents the practical model of a zener diode, where the zener impedance (Z_Z) is included. Since the actual voltage curve is not ideally vertical, a change in zener current (ΔI_Z) produces a small change in zener voltage (ΔV_Z), as illustrated in Figure (c).



Zener diode equivalent circuit models and the characteristic curve illustrating Z_Z.

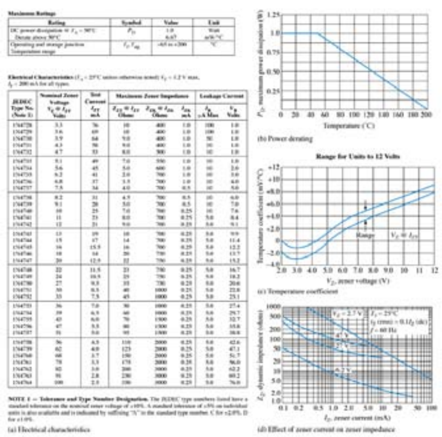
$$Z_Z = \frac{\Delta V_Z}{\Delta I_Z}$$

Ex 3-1 A zener diode exhibits a certain change in V_Z for a certain change in I_Z on a portion of the linear characteristic curve between I_{ZK} and I_{ZM} as illustrated in Figure. What is the zener impedance?



$$Z_Z = \frac{\Delta V_Z}{\Delta I_Z} = \frac{50mV}{5mV} = 10\Omega$$

Zener diode Data Sheet Information

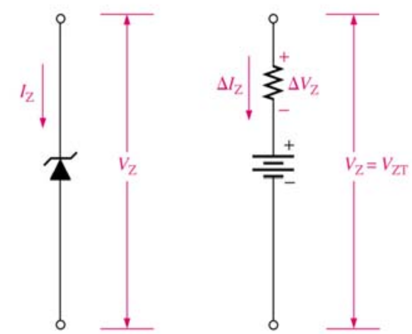


Partial data sheet for the 1N4728-1N4764 series 1 W zener diodes.

As with most devices, zener diodes have given characteristics such as temperature coefficients and power ratings that have to be considered. The data sheet provides this information.

- V_Z: zener voltage
- I_{ZT}: zener test current
- Z_{ZT}: zener Impedance
- I_{ZK}: zener knee current
- I_{ZM}: maximum zener current

Ex 3-2 A IN4736 zener diode has a Z_{ZT} of 3.5 Ω. The data sheet gives V_{ZT} = 6.8 V at I_{ZT} = 37 mA and I_{ZK} = 1 mA. What is the voltage across the zener terminals when the current is 50 mA? When the current is 25 mA?



$\Delta I_Z = I_Z - I_{ZT} = +13$ mA

$\Delta V_Z = \Delta I_Z Z_{ZT} = (13 \text{ mA})(3.5\ \Omega) = +45.5\text{mV}$

$V_Z = 6.8 \text{ V} + \Delta V_Z = 6.8 \text{ V} + 45.5 \text{ mV} = 6.85\text{V}$

$\Delta I_Z = -12$ mA

$\Delta V_Z = \Delta I_Z Z_{ZT} = (-12 \text{ mA})(3.5\ \Omega) = -42$ mV

$V_Z = 6.8 \text{ V} - \Delta V_Z = 6.8 \text{ V} - 42 \text{ mV} = 6.76\text{V}$

The **temperature coefficient** specifies the percent change in zener voltage for each °C change in temperature. For example, a 12 V zener diode with a positive temperature coefficient of 0.01%/°C will exhibit a 1.2 mV increase in V_Z when the junction temperature increases one Celsius degree. $\Delta V_Z = V_Z \times TC \times \Delta T$

Where V_Z is the nominal zener voltage at 25 °C, TC is the temperature coefficient, and ΔT is the change in temperature.

Ex 3-3 An 8.2 V zener diode (8.2 V at 25 °C) has a positive temperature coefficient of 0.05 %/°C. What is the zener voltage at 60 °C?

The change in zener voltage is

$$\Delta V_Z = V_Z \times TC \times \Delta T = (8.2 \text{ V})(0.05\ \%/^\circ\text{C})(60\ ^\circ\text{C} - 25\ ^\circ\text{C})$$

$$= (8.2 \text{ V})(0.0005/^\circ\text{C})(35\ ^\circ\text{C}) = 144 \text{ mV}$$

Notice that 0.05%/°C was converted to 0.0005/°C. The zener voltage at 60 °C is

$$V_Z + \Delta V_Z = 8.2 \text{ V} + 144 \text{ mV} = 8.34 \text{ V}$$

Zener Power Dissipating and Derating

Zener diodes are specified to operate at a maximum power called the maximum dc power dissipation, $P_{D(max)}$.

$$P_D = V_Z I_Z$$

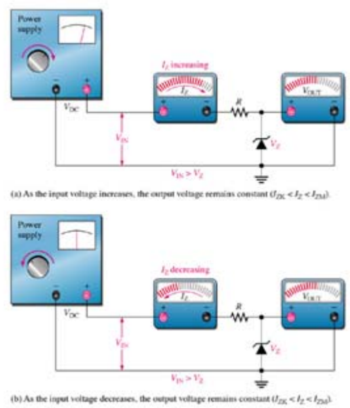
The maximum power dissipation of a zener diode is typically specified for temperature at or below a certain value (50 °C, for example). The derating factor is expressed in mW/°C. The maximum derated power can be determined with the following formula:

$$P_{D(derated)} = P_{D(max)} - (\text{mW}/^\circ\text{C})\Delta T$$

Ex 3-4 A certain zener diode has a maximum power rating of 400 mW at 50 °C and a derating factor of 3.2 mW/°C. Determine the maximum power the zener can dissipate at a temperature of 90 °C.

$$P_{D(derated)} = P_{D(max)} - (\text{mW}/^\circ\text{C})\Delta T$$
$$= 400 \text{ mW} - (3.2 \text{ mW}/^\circ\text{C})(90^\circ\text{C} - 50\ ^\circ\text{C})$$
$$= 400 \text{ mW} - 128 \text{ mW} = 272 \text{ mW}$$

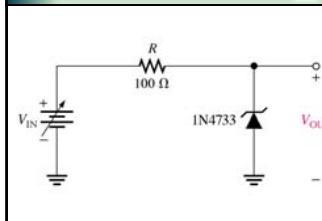
Zener Diode Applications –
Zener Regulation with a Varying Input Voltage



(a) As the input voltage increases, the output voltage remains constant ($I_{ZK} < I_Z < I_{ZM}$).

(b) As the input voltage decreases, the output voltage remains constant ($I_{ZK} < I_Z < I_{ZM}$).

Ex 3-5 Determine the minimum and the maximum input voltages that can be regulated by the zener diode in Figure.



From the data sheet in Figure, the following information for the IN4733 is obtained: $V_Z = 5.1$ V at $I_{ZT} = 49$ mA, $I_{ZK} = 1$ mA, and $Z_Z = 7\ \Omega$ at I_{ZT}.

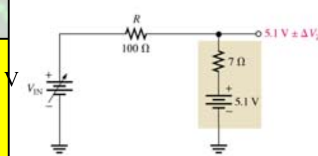
$V_{OUT} \approx 5.1\text{V} - \Delta V_Z = 5.1\text{ V} - (I_{ZT} - I_{ZK})Z_Z$
$= 5.1\text{ V} - (48\text{ mA})(7\ \Omega) = 5.1\text{ V} - 0.336\text{ V}$
$= 4.76\text{ V}$

$V_{IN(min)} = I_{ZK}R + V_{OUT}$
$= (1\text{ mA})(100\ \Omega) + 4.76\text{ V} = 4.86\text{ V}$

$$I_{ZM} = \frac{P_{D(max)}}{V_Z} = \frac{1W}{5.1V} = 196\,mA$$

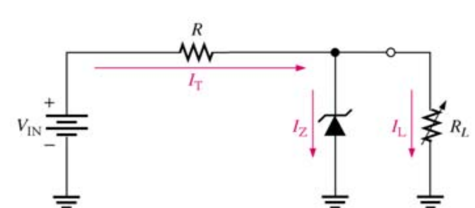
$V_{OUT} \approx 5.1\text{V} - \Delta V_Z = 5.1\text{ V} + (I_{ZM} - I_{ZT})Z_Z$
$= 5.1\text{ V} + (147\text{ mA})(7\ \Omega) = 5.1\text{ V} + 1.03\text{ V}$
$= 6.13\text{ V}$

$V_{IN(min)} = I_{ZM}R + V_{OUT}$
$= (196\text{ mA})(100\ \Omega) + 6.13\text{ V} = 25.7\text{ V}$

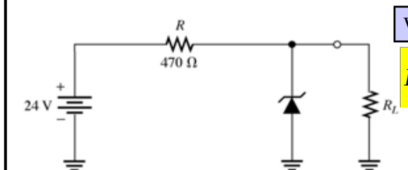


Zener Regulation with a Variable Load

In this simple illustration of zener regulation circuit, the zener diode will "adjust" its impedance based on varying input voltages and loads (R_L) to be able to maintain its designated zener voltage. ***Zener current will increase or decrease directly with voltage input changes***. The zener current will increase or decrease inversely with varying loads. Again, the zener has a finite range of operation.



Ex 3-6 Determine the minimum and the maximum load currents for which the zener diode in Figure will maintain regulation. What is the minimum R_L that can be used? $V_Z = 12$ V, $I_{ZK} = 1$ mA, and $I_{ZM} = 50$ mA. Assume $Z_Z = 0\ \Omega$ and V_Z remains a constant 12 V over the range of current values, for simplicity.



When $I_L = 0$ A ($R_L = \infty$), I_Z is maximum

$$I_{Z(max)} = I_T = \frac{V_{IN} - V_Z}{R}$$

$$= \frac{24\,V - 12\,V}{470\,\Omega} = 25.5\,mA$$

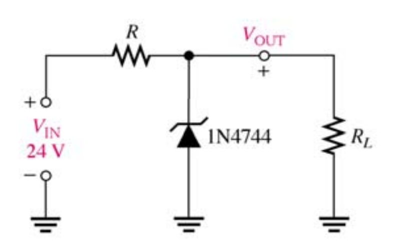
Since $I_{Z(max)}$ is less than I_{ZM}, 0 A is an acceptable minimum value for I_L because the zener can handle all of the 25.5 mA. **$I_{L(min)} = 0$ A**

The maximum value of I_L occurs when I_Z is minimum ($I_Z = I_{ZK}$),
$I_{L(max)} = I_T - I_{ZK} = 25.5\text{ mA} - 1\text{mA} = 24.5\text{ mA}$

The minimum value of RL is
$R_{L(min)} = V_Z/I_{L(max)} = 12\text{ V}/24.5\text{ mA} = 490\ \Omega$

Ex 3-7 For the circuit in Figure:

(a) Determine V_{OUT} at I_{ZK} and I_{ZM}.
(b) Calculate the value of R that should be used.
(c) Determine the minimum value of R_L that can be used.



(a) For I_{ZK}:

$V_{OUT} = V_Z = 15\text{ V} - \Delta I_Z Z_{ZT}$
$= 15\text{ V} - (I_{ZT} - I_{ZK})Z_{ZT}$
$= 15\text{ V} - (16.75\text{ mA})(14\Omega)$
$= 15\text{ V} - 0.235\text{ V} = 14.76\text{ V}$

Calculate the zener maximum current.
The power dissipation is 1 W.

$$I_{ZM} = \frac{P_{D(\max)}}{V_Z} = \frac{1W}{15V} = 66.7mA$$

For I_{ZM}:

$V_{OUT} = V_Z = 15\text{ V} + \Delta I_Z Z_{ZT} = 15\text{ V} + (I_{ZM} - I_{ZT})Z_{ZT}$
$= 15\text{ V} + (49.7\text{ mA})(14\Omega) = 15.7\text{ V}$

(b) The value of R is calculated for the maximum zener current that occurs when there is no load as shown in Figure (a).

$$R = \frac{V_{IN} - V_Z}{I_{ZM}} = \frac{24V - 15.7V}{66.7mA} = 124\Omega$$

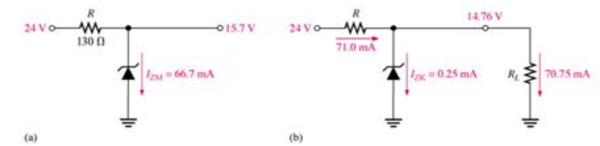
R = 130 Ω (nearest larger standard value).

(c) For the minimum load resistance (maximum load current), the zener current is minimum (I_{ZK} = 0.25 mA) as shown in Figure (b).

$$I_T = \frac{V_{IN} - V_{OUT}}{R} = \frac{24V - 14.76V}{130\Omega} = 71.0mA$$

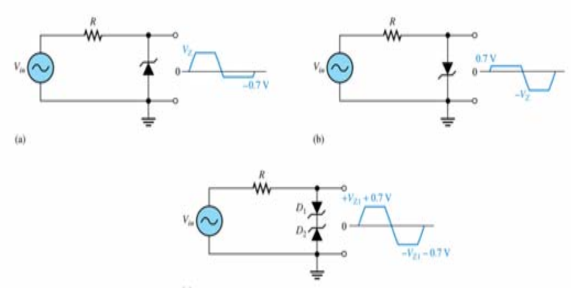
$$I_L = I_T - I_{ZK} = 71.0mA - 0.25mA = 70.75mA$$

$$R_{L(\min)} = \frac{V_{OUT}}{I_L} = \frac{14.76V}{70.75mA} = 209\Omega$$

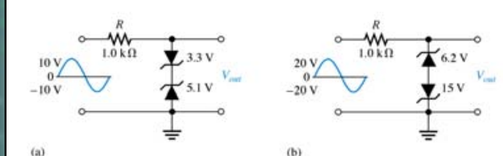


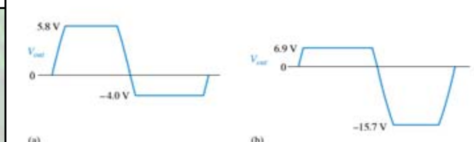
Zener Limiting

Zener diodes can used in ***ac applications to limit voltage swings to desired levels***. Part (a) shows a zener used to limit the positive peak of a signal voltage to the selected voltage. When the zener is turned around, as in part (b), the negative peak is limited by zener action and the positive voltage is limited to + 0.7 V.



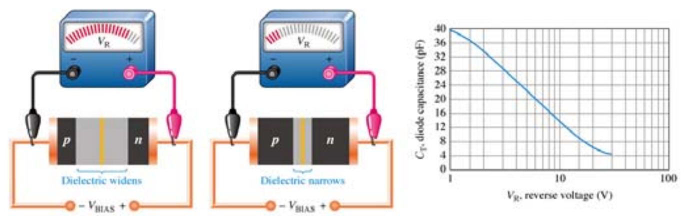
Ex 3-8 Determine the output voltage for each zener limiting circuit in Figure.





Varactor Diodes

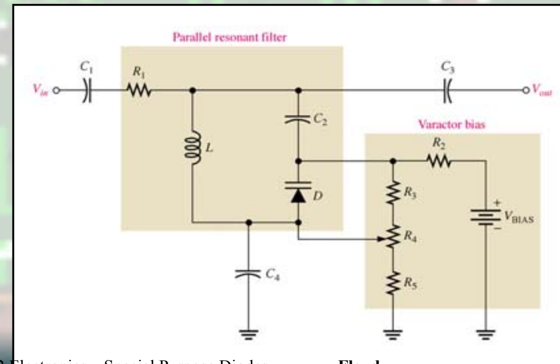
A **varactor diode** is best explained as a variable capacitor. Think of the depletion region a variable dielectric. The diode is placed in reverse bias. The dielectric is "adjusted" by bias changes.



(a) Greater reverse bias, less capacitance (b) Less reverse bias, greater capacitance (c) Graph of diode capacitance versus reverse voltage

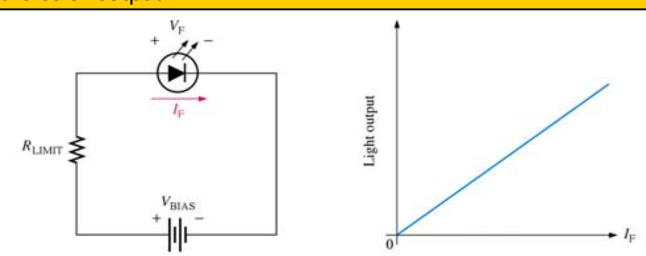
Varactor Diodes

The varactor diode can be useful in filter circuits as the adjustable component.



Optical Diodes

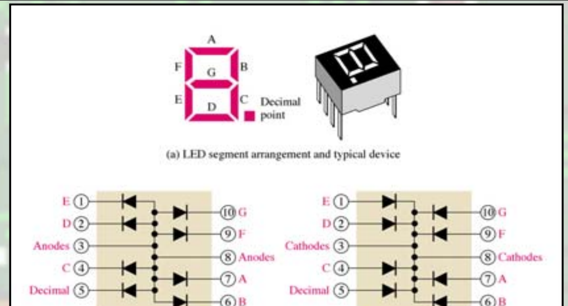
The **light-emitting diode** (LED) emits photons as visible light. It's purpose is for indication and other intelligible displays. Various impurities are added during the doping process to vary the color output.



(a) Forward-biased operation (b) General light output versus forward current

Optical Diodes

The seven segment display is an example of LEDs use for display of decimal digits.

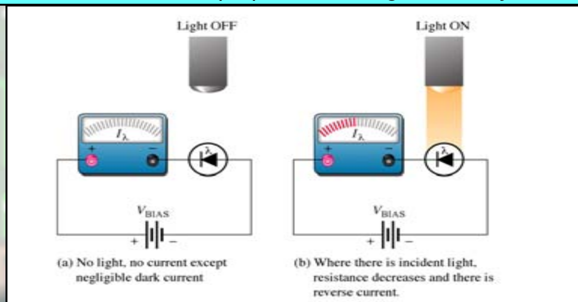


(a) LED segment arrangement and typical device

(b) Common anode (c) Common cathode

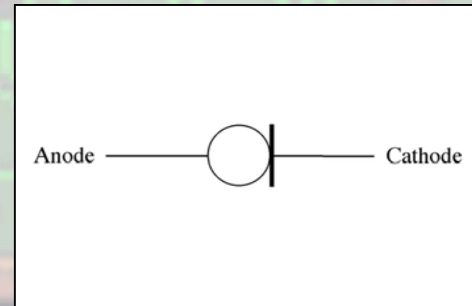
Optical Diodes

The **photodiode** is used to vary current by the amount of light that strikes it. It is placed in the circuit in reverse bias. As with most diodes when in reverse bias, no current flows when in reverse bias, but when light strikes the exposed junction through a tiny window, reverse current increases proportional to light intensity.



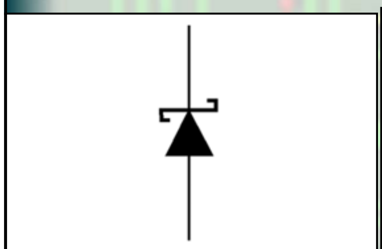
Other Diode Types

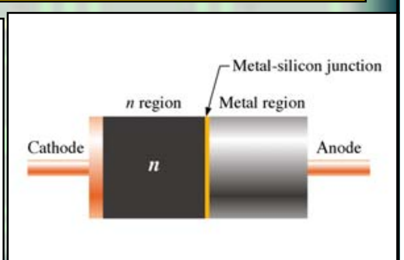
Current regulator diodes keeps a constant current value over a specified range of forward voltages ranging from about 1.5 V to 6 V.



Other Diode Types

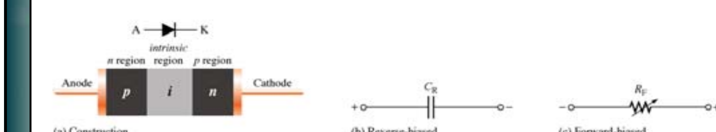
The **Schottky diode's** significant characteristic is it's fast switching speed. This is useful for high frequencies and digital applications. It is not a typical diode in the fact that it does not have a p-n junction, instead it consists of a heavily doped n-material and metal bound together.





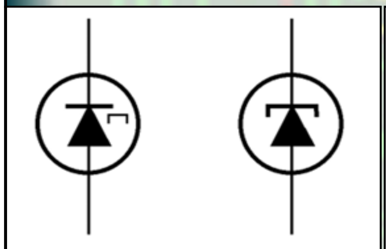
Other Diode Types

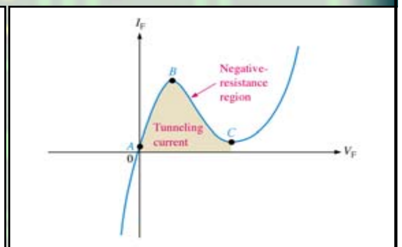
The ***pin* diode** is also used in mostly microwave frequency applications. It's variable forward series resistance characteristic is used for attenuation, modulation, and switching. In reverse bias exhibits a nearly constant capacitance.



Other Diode Types

The **step-recovery diode** is also used for fast switching applications. This is achieved by reduced doping at the junction.



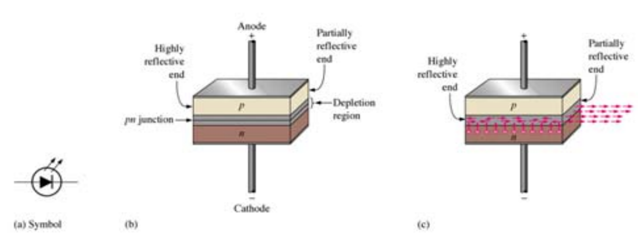


Other Diode Types

The **tunnel diode** has negative resistance. It will actually conduct well with low forward bias. With further increases in bias it reaches the negative resistance range where current will actually go down. This is achieved by heavily doped p and n materials that creates a very thin depletion region.

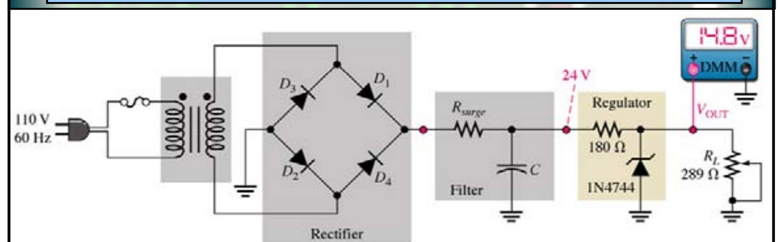
Other Diode Types

The **laser diode** (**l**ight **a**mplification by **s**timulated **e**mission of **r**adiation) produces a monochromatic (single color) light. Laser diodes in conjunction with photodiodes are used to retrieve data from compact discs.



Troubleshooting

Although precise power supplies typically use IC type regulators, zener diodes can be used alone as a voltage regulator. As with all troubleshooting techniques we must know what is normal.



(b) Correct output voltage with full load

A properly functioning zener will work to maintain the output voltage within certain limits despite changes in load.

EET1240/ET212 Electronics

Bipolar Junction Transistors

Electrical and Telecommunications Engineering Technology Department

Professor Jang

Prepared by textbook based on "Electronics Devices" by Floyd, Prentice Hall, 7th edition.

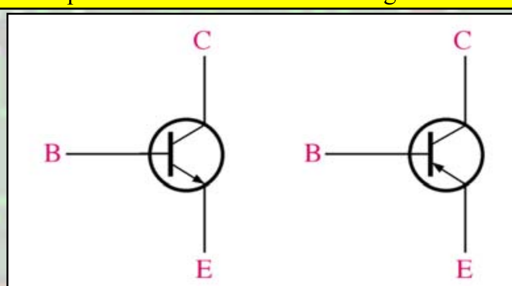
Objectives

- Introduction to Bipolar Junction Transistor (BJT)
- Basic Transistor Bias and Operation
- Parameters, Characteristics and Transistor Circuits
- Amplifier or Switch

Key Words: BJT, Bias, Transistor, Amplifier, Switch

Introduction

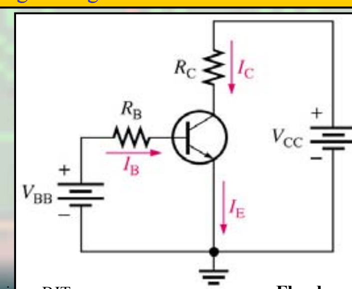
A **transistor** is a device which can be used as either an **amplifier** or a **switch**. Let's first consider its operation in a more simple view as a current controlling device.



(a) *npn* (b) *pnp*

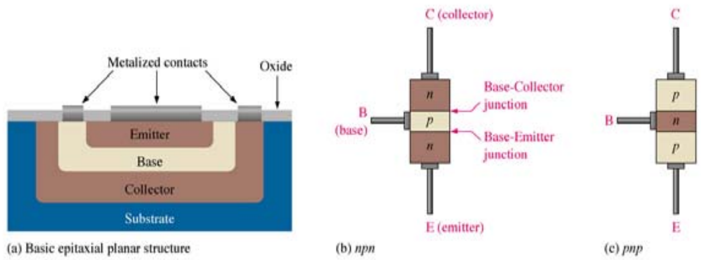
Basic Transistor Operation

Look at this one circuit as two separate circuits, the base-emitter(left side) circuit and the collector-emitter(right side) circuit. Note that the emitter leg serves as a conductor for both circuits.The amount of current flow in the base-emitter circuit controls the amount of current that flows in the collector circuit. Small changes in base-emitter current yields a large change in collector-current.



Transistor Structure

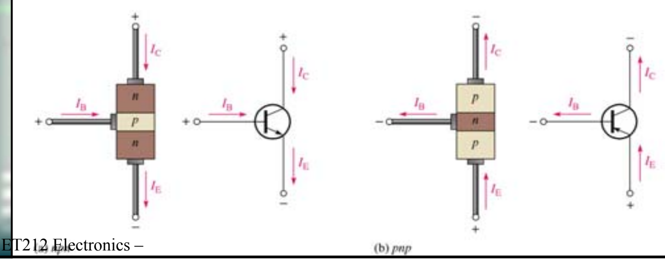
The **BJT (bipolar junction transistor)** is constructed with three doped semiconductor regions separated by two pn junctions, as shown in Figure (a). The three regions are called **emitter**, **base**, and **collector**. Physical representations of the two types of BJTs are shown in Figure (b) and (c). One type consists of two n regions separated by a *p* regions (*npn*), and other type consists of two p regions separated by an *n* region (*pnp*).



Transistor Currents

The directions of the currents in both npn and pnp transistors and their schematic symbol are shown in Figure (a) and (b). Notice that the arrow on the emitter of the transistor symbols points in the direction of conventional current. These diagrams show that the emitter current (**I_E**) is the sum of the collector current (**I_C**) and the base current (**I_B**), expressed as follows:

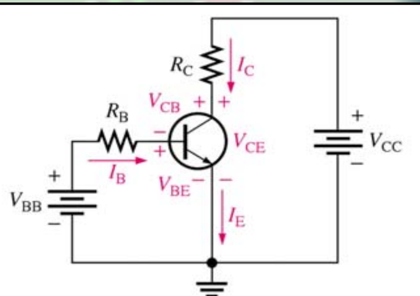
$$I_E = I_C + I_B$$

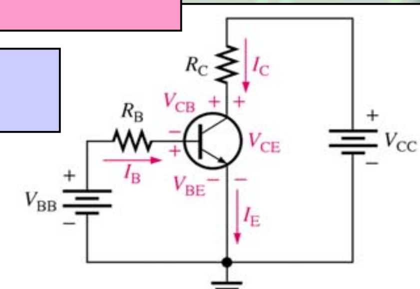


Transistor Characteristics and Parameters

Figure shows the proper bias arrangement for npn **transistor** for active operation as an amplifier.Notice that the base-emitter (**BE**) junction is forward-biased and the base-collector (**BC**) junction is reverse-biased. As previously discussed, base-emitter current changes yields large changes in collector-emitter current. The factor of this change is called ***beta***(β).

$$\beta = I_C/I_B$$



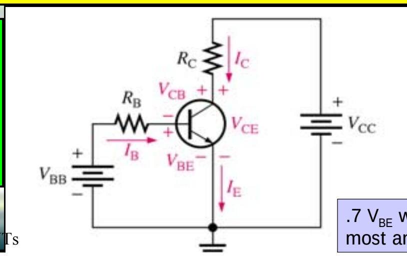


Transistor Characteristics and Parameters

Analysis of this transistor circuit to predict the dc voltages and currents requires use of Ohm's law, Kirchhoff's voltage law and the beta for the transistor.

Application of these laws begins with the base circuit to determine the amount of base current. Using Kichhoff's voltage law, subtract the .7 V_{BE} and the remaining voltage is dropped across R_B. Determining the current for the base with this information is a matter of applying of Ohm's law. $\mathbf{V_{R_B}/R_B = I_B}$

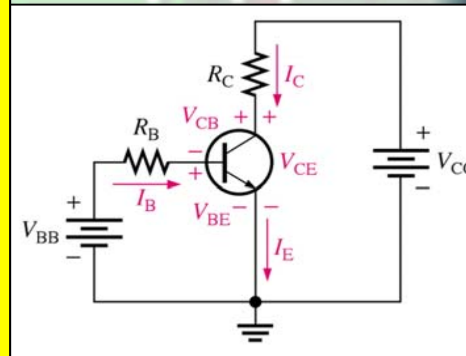
The collector current is determined by multiplying the base current by beta.



.7 V_{BE} will be used in most analysis examples.

Transistor Characteristics and Parameters

What we ultimately determine by use of Kirchhoff's voltage law for series circuits is that in the base circuit V_{BB} is distributed across the base-emitter junction and R_B in the base circuit. In the collector circuit we determine that V_{CC} is distributed proportionally across R_C and the transistor(V_{CE}).



Current and Voltage Analysis

There are three key dc voltages and three key dc currents to be considered. Note that these measurements are important for troubleshooting.

I_B: dc base current

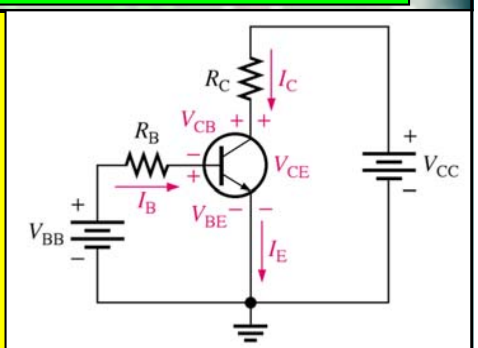
I_E: dc emitter current

I_C: dc collector current

V_{BE}: dc voltage across base-emitter junction

V_{CB}: dc voltage across collector-base junction

V_{CE}: dc voltage from collector to emitter



Current and Voltage Analysis-continued

When the base-emitter junction is forward-biased,

$\mathbf{V_{BE} \cong 0.7\ V}$

$\mathbf{V_{R_B} = I_B R_B}$: by Ohm's law

$\mathbf{I_B R_B = V_{BB} - V_{BE}}$: substituting for V_{RB}

$\mathbf{I_B = (V_{BB} - V_{BE}) / R_B}$: solving for I_B

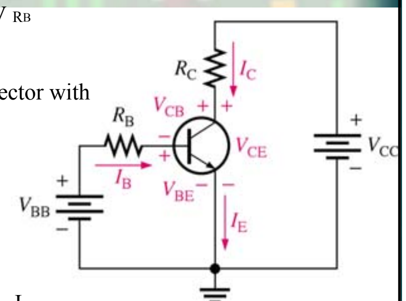
$\mathbf{V_{CE} = V_{CC} - V_{Rc}}$: voltage at the collector with respect to emitter

$\mathbf{V_{Rc} = I_C R_C}$

$\mathbf{V_{CE} = V_{CC} - I_C R_C}$

The voltage across the reverse-biased collector-base junction

$\mathbf{V_{CB} = V_{CE} - V_{BE}}$ where $I_C = \beta_{DC} I_B$



Ex 3-2 Determine I_B, I_C, V_{BE}, V_{CE}, and V_{CB} in the circuit of Figure. The transistor has a $\beta_{DC} = 150$.

When the base-emitter junction is forward-biased,

$V_{BE} \cong 0.7\ V$

$I_B = (V_{BB} - V_{BE}) / R_B$

$= (5\ V - 0.7\ V) / 10\ k\Omega = 430\ \mu A$

$I_C = \beta_{DC} I_B$

$= (150)(430\ \mu A)$

$= 64.5\ mA$

$I_E = I_C + I_B$

$= 64.5\ mA + 430\ \mu A$

$= 64.9\ mA$

$V_{CE} = V_{CC} - I_C R_C$

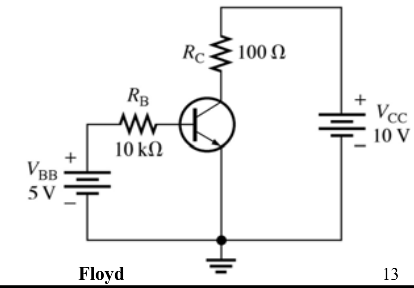
$= 10\ V - (64.5\ mA)(100\ \Omega)$

$= 3.55\ V$

$V_{CB} = V_{CE} - V_{BE}$

$= 3.55\ V - 0.7\ V$

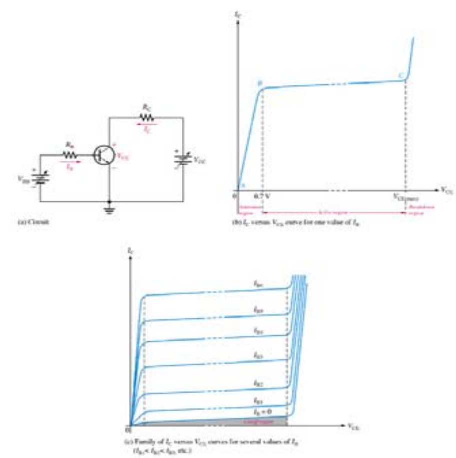
$= 2.85\ V$



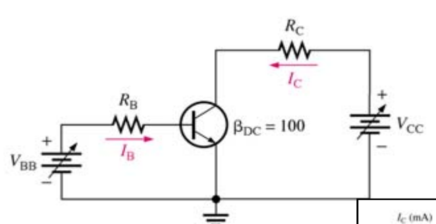
Floyd

Collector Characteristic Curve

Collector characteristic curves gives a graphical illustration of the relationship of collector current and V_{CE} with specified amounts of base current. With greater increases of V_{CC}, V_{CE} continues to increase until it reaches breakdown, but the current remains about the same in the **linear** region from .7V to the breakdown voltage.



Ex 3-3 Sketch an ideal family of collector curves for for the circuit in Figure for $I_B = 5\ \mu A$ increment. Assume $\beta_{DC} = 100$ and that V_{CE} does not exceed breakdown.

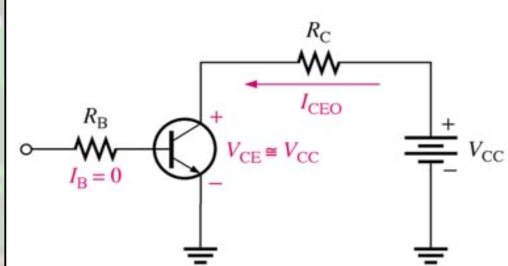


$I_C = \beta_{DC} I_B$

I_B	I_C
5 µA	0.5 mA
10 µA	1.0 mA
15 µA	1.5 mA
20 µA	2.0 mA
25 µA	2.5 mA

Transistor Characteristics and Parameters-Cutoff

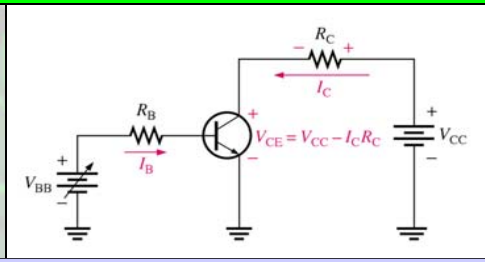
With no I_B the transistor is in the **cutoff** region and just as the name implies there is practically no current flow in the collector part of the circuit. With the transistor in a cutoff state the the full V_{CC} can be measured across the collector and emitter(V_{CE})



Cutoff: Collector leakage current (I_{CEO}) is extremely small and is usually neglected. Base-emitter and base-collector junctions are reverse-biased.

Transistor Characteristics and Parameters - **Saturation**

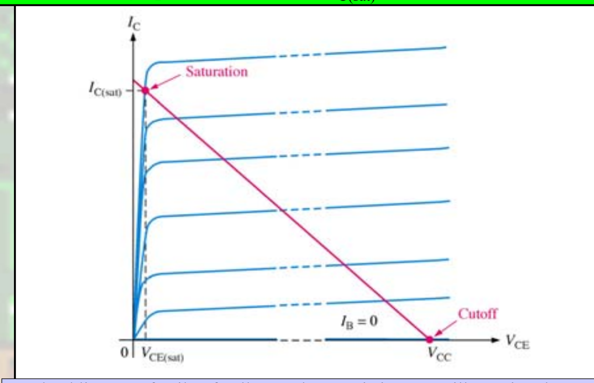
Once this maximum is reached, the transistor is said to be in **saturation**. Note that saturation can be determined by application of Ohm's law. $I_{C(sat)} = V_{CC}/R_C$ The measured voltage across this now seemingly "shorted" collector and emitter is 0V.



Saturation: As I_B increases due to increasing V_{BB}, I_C also increases and V_{CE} decreases due to the increased voltage drop across R_C. When the transistor reaches saturation, I_C can increase no further regardless of further increase in I_B. Base-emitter and base-collector junctions are forward-biased.

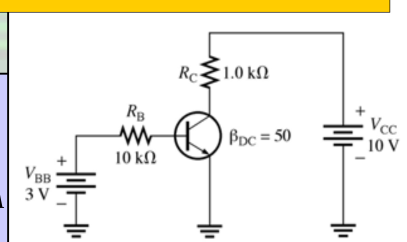
Transistor Characteristics and Parameters - **DC Load Line**

The **dc load line** graphically illustrates $I_{C(sat)}$ and Cutoff for a transistor.



DC load line on a family of collector characteristic curves illustrating the cutoff and saturation conditions.

Ex 3-4 Determine whether or not the transistors in Figure is in saturation. Assume $V_{CE(sat)} = 0.2$ V.



First, determine $I_{C(sat)}$

$$I_{C(sat)} = \frac{V_{CC} - V_{CE(sat)}}{R_C} = \frac{10V - 0.2V}{1.0k\Omega} = 9.8\ mA$$

Now, see if I_B is large enough to produce $I_{C(sat)}$.

$$I_B = \frac{V_{BB} - V_{BE}}{R_B} = \frac{3V - 0.7V}{10k\Omega} = \frac{2.3V}{10\,k\Omega} = 0.23\ mA$$

$$I_C = \beta_{DC} I_B = (50)(0.23\,mA) = 11.5\ mA$$

Transistor Characteristics and Parameters – **Maximum Transistor Ratings**

A transistor has limitations on its operation. The product of V_{CE} and I_C cannot be maximum at the same time. If V_{CE} is maximum, I_C can be calculated as

$$I_C = \frac{P_{D(max)}}{V_{CE}}$$

Ex 4-5 A certain transistor is to be operated with $V_{CE} = 6$ V. If its maximum power rating is 250 mW, what is the most collector current that it can handle?

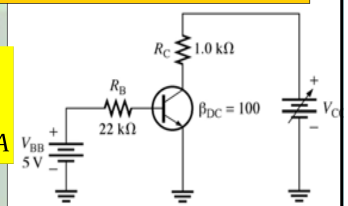
$$I_C = \frac{P_{D(max)}}{V_{CE}} = \frac{250\,mW}{6V} = 41.7\ mA$$

Ex 3-5 The transistor in Figure has the following maximum ratings: $P_{D(max)}$ = 800 mW, $V_{CE(max)}$ = 15 V, and $I_{C(max)}$ = 100 mA. Determine the maximum value to which V_{CC} can be adjusted without exceeding a rating. Which rating would be exceeded first?

First, find I_B so that you can determine I_C.

$$I_B = \frac{V_{BB} - V_{BE}}{R_B} = \frac{5V - 0.7V}{22k\Omega} = 195\mu A$$

$$I_C = \beta_{DC} I_B = (100)(195\mu A) = 19.5mA$$



The voltage drop across R_C is.

$V_{Rc} = I_C R_C$ = (19.5 mA)(1.0 kΩ) = 19.5 V
$V_{Rc} = V_{CC} - V_{CE}$ when $V_{CE} = V_{CE(max)}$ = 15 V
$V_{CC(max)} = V_{CE(max)} + V_{Rc}$ = 15 V + 19.5 V = 34.5 V

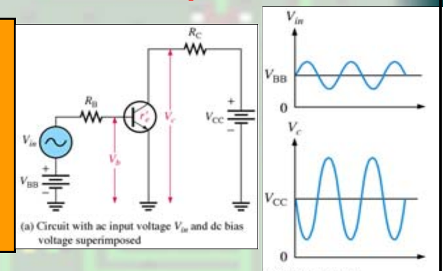
$P_D = V_{CE(max)} I_C$ = (15V)(19.5mA) = 293 mW

$V_{CE(max)}$ will be exceeded first because the entire supply voltage, V_{CC} will be dropped across the transistor.

The Transistor as an Amplifier

Amplification of a relatively small ac voltage can be had by placing the ac signal source in the base circuit.

Recall that small changes in the base current circuit causes large changes in collector current circuit.

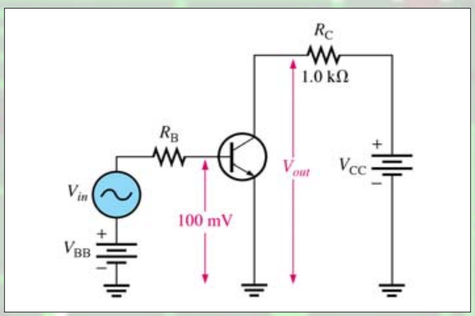


(a) Circuit with ac input voltage V_{in} and dc bias voltage superimposed

(b) Waveforms

The ac emitter current : $I_e \approx I_c = V_b/r'_e$
The ac collector voltage : $V_c = I_c R_c$
Since $I_c \approx I_e$, the ac collector voltage : $V_c \approx I_e R_c$
The ratio of V_c to V_b is the ac voltage gain : $A_v = V_c/V_b$
Substituting $I_e R_c$ for V_c and $I_e r'_e$ for V_b : $A_v = V_c/V_b \approx I_c R_c/I_e r'_e$
The I_e terms cancel : $A_v \approx R_c/r'_e$

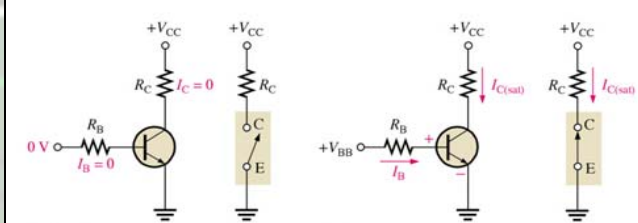
Ex 3-6 Determine the voltage gain and the ac output voltage in Figure if r'_e = 50 Ω.



The voltage gain : $A_v \approx R_c/r'_e$ = 1.0 kΩ/50 Ω = 20
The ac output voltage : $A_v V_b$ = (20)(100 mV) = 2 V

The Transistor as a Switch

A transistor when used as a switch is simply being biased so that it is in **cutoff (switched off)** or **saturation (switched on).** Remember that the V_{CE} in cutoff is V_{CC} and 0V in saturation.



(a) Cutoff — open switch

(b) Saturation — closed switch

Conditions in Cutoff & Saturation

A transistor is in the cutoff region when the base-emitter junction is not forward-biased. All of the current are zero, and V_{CE} is equal to V_{CC}

$$V_{CE(cutoff)} = V_{CC}$$

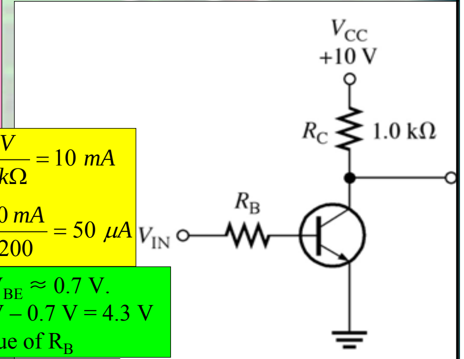
When the base-emitter junction is forward-biased and there is enough base current to produce a maximum collector current, the transistor is saturated. The formula for collector saturation current is

$$I_{C(sat)} = \frac{V_{CC} - V_{CE(sat)}}{R_C}$$

The minimum value of base current needed to produce saturation is

$$I_{B(min)} = \frac{I_{C(sat)}}{\beta_{DC}}$$

Ex 3-7 (a) For the transistor circuit in Figure, what is V_{CE} when $V_{IN} = 0$ V?
(b) What minimum value of I_B is required to saturate this transistor if β_{DC} is 200? Neglect $V_{CE(sat)}$.
(c) Calculate the maximum value of R_B when $V_{IN} = 5$ V.



(a) When $V_{IN} = 0$ V
$V_{CE} = V_{CC} = 10$ V

(b) Since $V_{CE(sat)}$ is neglected,

$$I_{C(sat)} = \frac{V_{CC}}{R_C} = \frac{10\,V}{1.0\,k\Omega} = 10\ mA$$

$$I_{B(min)} = \frac{I_{C(sat)}}{\beta_{DC}} = \frac{10\ mA}{200} = 50\ \mu A$$

(c) When the transistor is on, $V_{BE} \approx 0.7$ V.
$V_{R_B} = V_{IN} - V_{BE} \approx 5\text{ V} - 0.7\text{ V} = 4.3$ V
Calculate the maximum value of R_B

$$R_{B(max)} = \frac{V_{R_B}}{I_{B(min)}} = \frac{4.3V}{50\ \mu A} = 86\ k\Omega$$

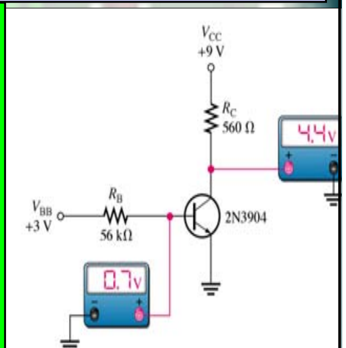
Troubleshooting

Opens in the external resistors or connections of the base or the circuit collector circuit would cause current to cease in the collector and the voltage measurements would indicate this.

Internal opens within the transistor itself could also cause transistor operation to cease.

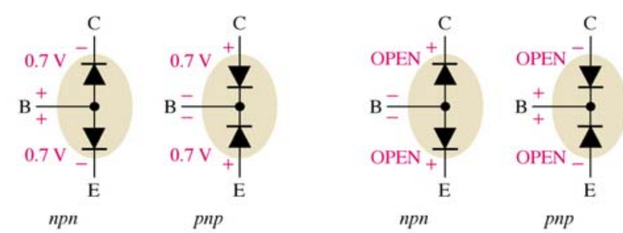
Erroneous voltage measurements that are typically low are a result of point that is not "solidly connected". This called a **floating point**. This is typically indicative of an open.

More in-depth discussion of typical failures are discussed within the textbook.



Troubleshooting

Testing a transistor can be viewed more simply if you view it as testing two diode junctions. Forward bias having low resistance and reverse bias having infinite resistance.



(a) Both junctions should read 0.7 V ± 0.2 V when forward-biased.

(b) Both junctions should ideally read OPEN when reverse-biased.

EET1240/ET212 Electronics

Field Effect Transistor (FET)

Electrical and Telecommunications Engineering Technology Departmnet

Professor Jang

Prepared by textbook based on "Electronics Devices" by Floyd, Prentice Hall, 7th edition.

Outlines

- Introduction to Field Effect Transistors (FET)
- JFET Parameters
- Biasing JFETs
- Metal Oxide Semiconductor Field Effect Transistors (MOSFET)
- Biasing MOSFET

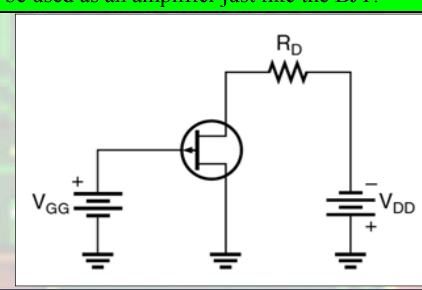
Key Words: FET, JFET, Voltage Controlled Device, Pinch Off, Cut Off, MOSFET

FET - Introduction

BJTs (bipolar junction transistors) were covered in previous chapters. Now we will discuss the second major type of transistor, the **FET** (field-effect transistor). Recall that a BJT is a current-controlled device; that is, the base current controls the amount of collector current. A FET is different. It is a **voltage-controlled device**, where the voltage between two of the terminal (gate and source) controls the current through the device. The FET's major advantage over the BJT is high input resistance. Overall the purpose of the FET is the same as the BJT.

The JFET

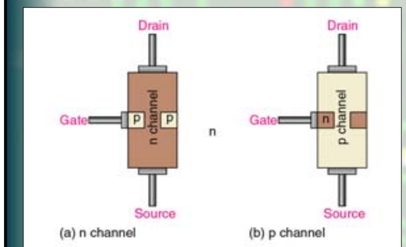
The **junction field effect transistor**, like a BJT, controls current flow. The difference is the way this is accomplished. The JFET uses **voltage to control the current flow**. As you will recall the transistor uses current flow through the base-emitter junction to control current. JFETs can be used as an amplifier just like the BJT.



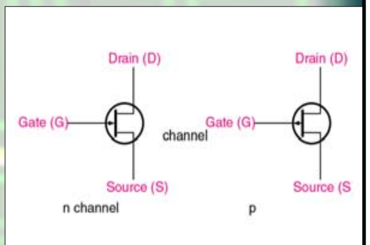
V_{GG} voltage levels control current flow in the V_{DD}, R_D circuit.

The JFET

Figure (a) shows the basic structure of an n-channel **JFET** (junction field-effect transistor). Wire leads are connected to each end of n-channel; the **drain** is at the upper end, and the **source** is at the lower end. Two p-type regions are diffused in the n-channel, and both p-type regions are connected to the **gate** lead.



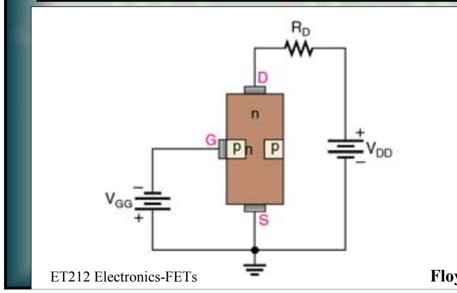
A representation of the basic structure of the two types of JFET.



JFET schematic symbols.

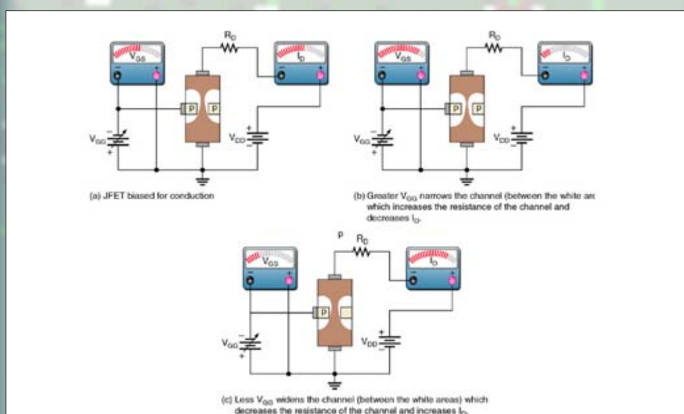
The JFET – Basic Operation

Figure shows dc bias voltages applied to an channel device. V_{DD} provides a drain-to-source voltage and supplies current from drain to source. The current is controlled by a field that is developed by the reverse biased gate-source junction (gate is connected to both sides). With more V_{GG} (reverse bias) the field (in white) grows larger. This field or resistance limits the amount of current flow through R_D.



The JFET is always operated with the gate-source pn junction reverse-biased.

The JFET – Basic Operation

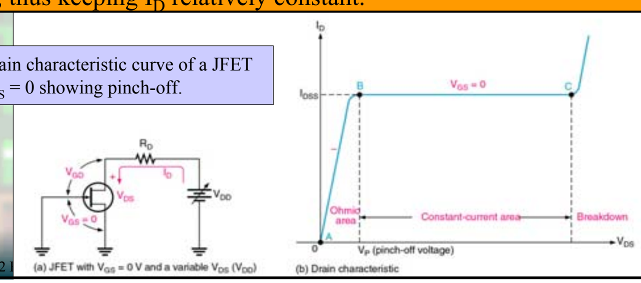


Effects of V_{GS} on channel width, resistance, and drain current ($V_{GG} = V_{GS}$).

JFET Characteristics and Parameters

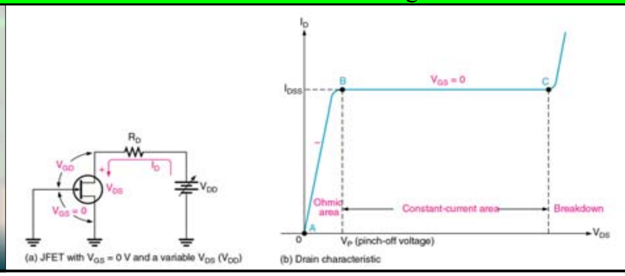
Let's first take a look at the effects with a $V_{GS} = 0V$. I_D increases proportionally with increases of V_{DD} (V_{DS} increases as V_{DD} is increased). This is called the ohmic region (point A to B) because V_{DS} and I_D are related by Ohm's law. As V_{DS} increases from point B to point C, the reverse-bias voltage from gate to drain (V_{GD}) produces a depletion region large enough to offset the increase in V_{DS}, thus keeping I_D relatively constant.

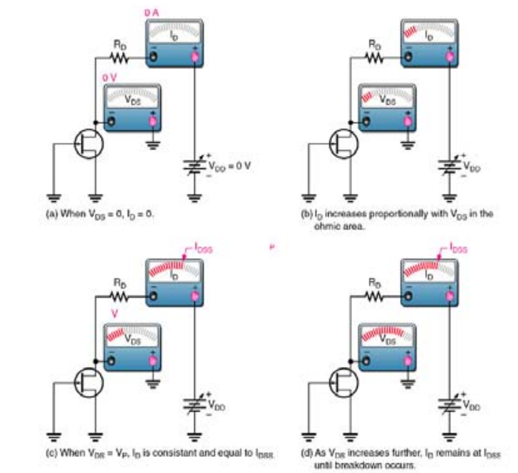
The drain characteristic curve of a JFET for $V_{GS} = 0$ showing pinch-off.



JFET Characteristics and Parameters – Pinch-Off Voltage

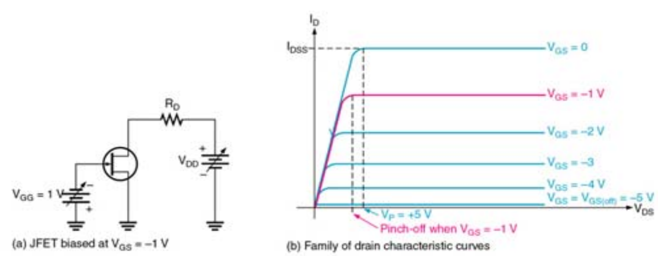
The point when I_D ceases to increase regardless of V_{DD} increases is called the **pinch-off voltage** (point B). This current is called maximum drain current (I_{DSS}). Breakdown (point C) is reached when too much voltage is applied. This of course undesirable, so JFETs operation is always well below this value. Because breakdown can result in irreversible damage to the device.





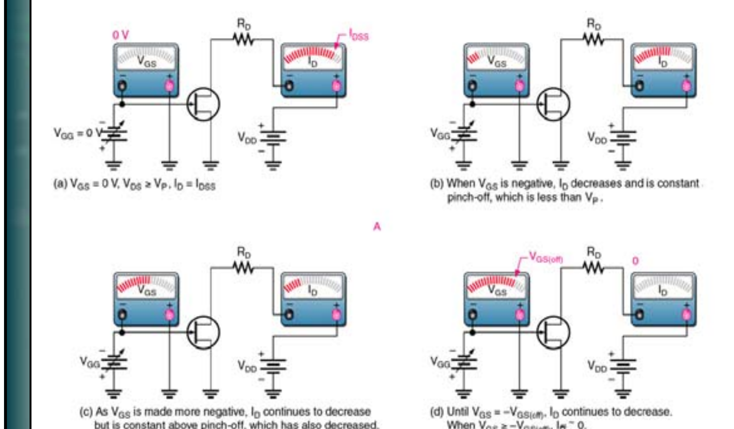
JFET Characteristics and Parameters – V_{GS} Controls I_D

From this set of curves you can see with increased voltage applied to the gate the I_D is limited and of course the pinch-off voltage is lowered as well. Notice that **I_D decreases as the magnitude of V_{GS} is increased** to larger negative values because of the narrowing of the channel.



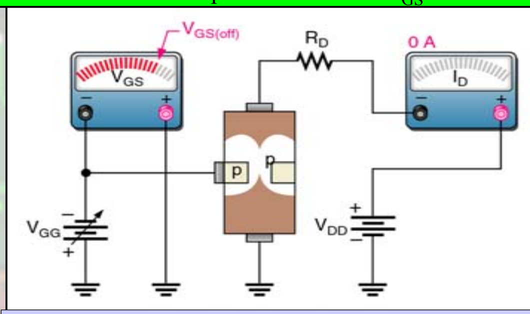
Pinch-off occurs at a lower V_{DS} as V_{GS} is increased to more negative values.

JFET Characteristics and Parameters – V_{GS} Controls I_D



JFET Characteristics and Parameters – Cutoff Voltage

We know that as V_{GS} is increased I_D will decrease. The value of V_{GS} that makes I_D approximately zero is the **cutoff voltage** **($V_{GS(off)}$)**. The field (in white) grows such that it allows practically no current to flow through. The JFET must be operated between $V_{GS} = 0$ and $V_{GS(off)}$.

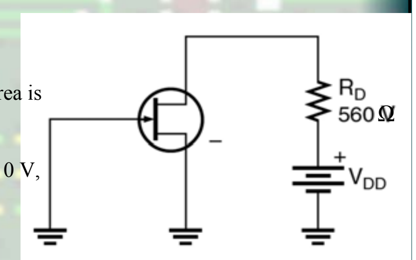


It is interesting to note that pinch-off voltage (V_P) and cutoff voltage ($V_{GS(off)}$) are both the same value only opposite polarity.

Comparison of Pinch-Off and Cutoff

As you have seen, there is a difference between pinch-off and cutoff. There is also a connection. V_P is the value of V_{DS} at which the drain current becomes constant and is always measured at $V_{GS} = 0$ V. However, pinch-off occurs for V_{DS} values less than V_P when V_{GS} is nonzero. So, although V_P is a constant, the minimum value of V_{DS} at which I_D becomes constant varies with V_{GS}. **$V_{GS(off)}$ and V_P are always equal in magnitude but opposite in sign.**

Ex. 7-1 For the JFET in Figure, $V_{GS(off)} = -4$ V and $I_{DSS} = 12$ mA. Determine the *minimum* value of V_{DD} required to put the device in the constant-current area of operation.



Since $V_{GS(off)} = -4$ V, $V_P = 4$ V.

The minimum value of V_{DS} for the JFET to be in its constant-current area is

$$V_{DS} = V_P = 4 \text{ V}$$

In the constant-current area with $V_{GS} = 0$ V,

$$I_D = I_{DSS} = 12 \text{ mA}$$

The drop across the drain resistor is

$$V_{RD} = I_D R_D = (12 \text{ mA})(560\Omega) = 6.72 \text{ V}$$

Apply Kirchhoff's law around the drain circuit.

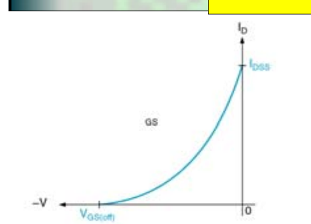
$$V_{DD} = V_{DS} + V_{RD} = 4 \text{ V} + 6.72 \text{ V} = 10.7 \text{ V}$$

This is the value of V_{DD} to make $V_{DS} = V_P$ and put the device in the constant-current area.

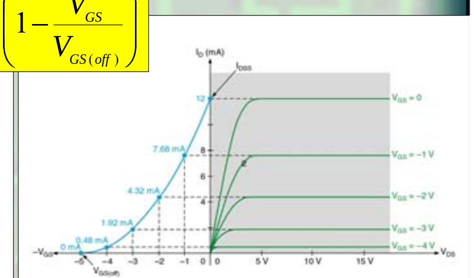
JFET Characteristics and Parameters – JFET Transfer Characteristic Curve

The transfer characteristic curve illustrates the control V_{GS} has on I_D from cutoff ($V_{GS(off)}$) to pinch-off (V_P). A JFET transfer characteristic curve is nearly parabolic in shape and can be expressed as

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$



JFET transfer characteristic curve (*n*-channel).



Example of the development of an *n*-channel JFET transfer characteristic curve (blue) from the JFET drain characteristic curves (green).

Ex. 7-2 A particular p-channel JFET has a $V_{GS(off)}$ = + 4 V. What is I_D when V_{GS} = + 6 V? Ans. I_D remains 0.

Ex. 7-3 The data sheet for a 2N5459 JFET indicates that typically I_{DSS} = 9 mA and $V_{GS(off)}$ = - 8 V (maximum). Using these values, determine the drain current for V_{GS} = 0 V, -1 V, and – 4 V.

For V_{GS} = 0 V,

$I_D = I_{DSS}$ = 9 mA

For V_{GS} = - 1 V,

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_{GS(off)}}\right)^2 = (9mA)\left(1-\frac{-1V}{-8V}\right)^2$$

$$= (9mA)(1-0.125)^2 = (9mA)(0.766) = 6.89mA$$

For V_{GS} = - 4 V,

$$I_D = (9mA)\left(1-\frac{-4V}{-8V}\right)^2 = (9mA)(1-0.5)^2 = (9mA)(0.25) = 2.25mA$$

JFET Biasing

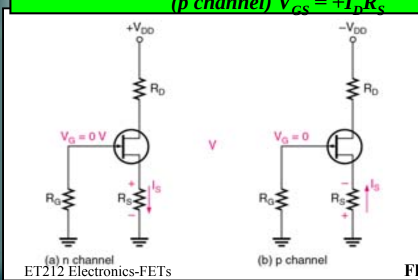
Just as we learned that the bi-polar junction transistor must be biased for proper operation, the JFET too must be biased for operation. Let's look at some of the methods for biasing JFETs. In most cases the **ideal Q-point** will be the middle of the transfer characteristic curve which is about half of the I_{DSS}. The purpose of biasing is to select the proper dc gate-to-source voltage to establish a desired value of drain current and, thus, a proper Q-point.

JFETBi asing – Self-Bias

Self-bias is the most common type of biasing method for JFETs. Notice there is no voltage applied to the gate. The voltage to ground from here will always be V_G = 0V. However, the voltage from gate to source (V_{GS}) will be negative for n channel and positive for p channel keeping the junction reverse biased. This voltage can be determined by the formulas below. $I_D = I_S$ for all JFET circuits.

(n channel) $V_{GS} = V_G - V_S = -I_D R_S$

(p channel) $V_{GS} = +I_D R_S$



$V_D = V_{DD} - I_D R_D$

$V_{DS} = V_D - V_S$
$= V_{DD} - I_D(R_D + R_S)$
where $V_S = I_D R_S$

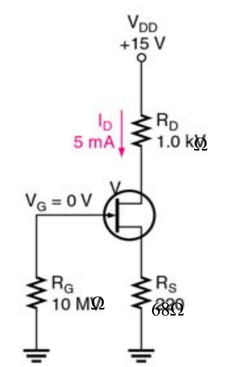
Ex. 7-4 Find V_{DS} and V_{GS} in Figure. For the particular JFET in this circuit, the internal parameter values such as g_m, $V_{GS(off)}$, and I_{DSS} are such that a drain current (I_D) of approximately 5 mA is produced. Another JFET, even of the same type, may not produce the same results when connected in this circuit due the variations in parameter values.

$V_S = I_D R_S$ = (5 mA)(68Ω) = 0.34 V

$V_D = V_{DD} - I_D R_D$ = 15 V – (5 mA)(1.0kΩ)
= 15 V – 5 V = 10 V

Therefore,
$V_{DS} = V_D - V_S$ = 10 V – 0.34 V = 9.66 V

Since V_G = 0 V,
$V_{GS} = V_G - V_S$ = 0 V – 0.34 V = – 0.34V



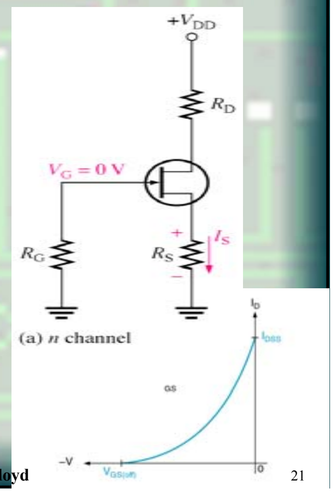
JFET Biasing – Setting the Q-point of a Self-Biased JFET

Setting the Q-point requires us to determine a value of R_S that will give us the desired I_D and V_{GS}. The formula below shows the relationship.

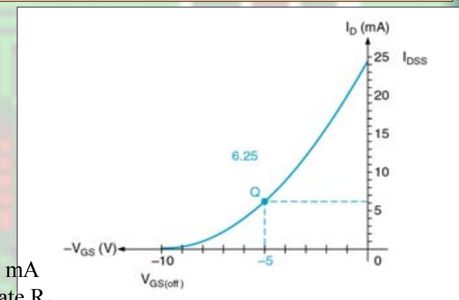
$$R_S = | V_{GS} / I_D |$$

To be able to do that we must first determine the V_{GS} and I_D from the either the transfer characteristic curve or more practically from the formula below. The data sheet provides the I_{DSS} and $V_{GS(off)}$. V_{GS} is the desired voltage to set the bias.

$$I_D = I_{DSS}(1 - V_{GS} / V_{GS(off)})^2$$



Ex. 7-5 Determine the value of R_S required to self-bias an n-channel JFET that has the transfer characteristic curve shown in Figure at V_{GS} = - 5 V.



From the graph, I_D = 6.25 mA when V_{GS} = - 5 V. Calculate R_S.

$$R_S = \left|\frac{V_{GS}}{I_D}\right| = \frac{5V}{6.25mA} = 800\Omega$$

Ex. 7-6 Determine the value of R_S required to self-bias an p-channel JFET with I_{DSS} = 25 mA and $V_{GS(off)}$ = 15 V. V_{GS} is to be 5 V.

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2 = (25\,mA)\left(1 - \frac{5V}{15V}\right)^2$$

$$= (25mA)(1 - 0.333)^2 = 11.1\,mA$$

Now, determine R_S.

$$R_S = \left|\frac{V_{GS}}{I_D}\right| = \frac{5V}{11.1\,mA} = 450\,\Omega$$

JFET Biasing – Voltage-Divider Bias

Voltage-divider bias can also be used to bias a JFET. R_1 and R_2 are used to keep the gate-source junction in reverse bias. Operation is no different from self-bias. Determining I_D, V_{GS} for a JFET voltage-divider circuit with V_D given can be calculated with the formulas below.

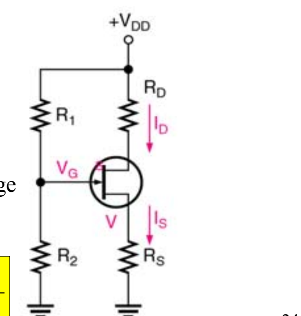
$V_S = I_D R_S$: Source voltage

$V_G = \left(\frac{R_2}{R_1 + R_2}\right) V_{DD}$: Gate voltage

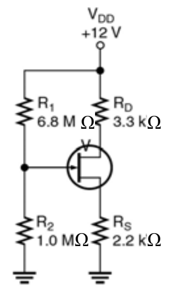
$V_{GS} = V_G - V_S$: Gate-to-source voltage

$I_D = \frac{V_S}{R_S}$: Drain current

$$I_D = \frac{V_G - V_{GS}}{R_S}$$



Ex. 7-7 Determine I_D and V_{GS} for the JFET with voltage-divider bias in Figure, given that for this particular JFET the internal parameter values are such that $V_D \approx 7$ V.



$$I_D = \frac{V_{DD} - V_D}{R_D} = \frac{12V - 7V}{3.3k\Omega} = \frac{5V}{3.3k\Omega} = 1.52mA$$

Calculate the gate-to-source voltage as follows:

$$V_S = I_D R_S = (1.52mA)(2.2k\Omega) = 3.34V$$

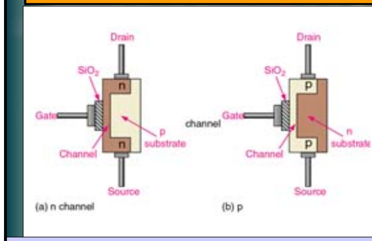
$$V_G = \left(\frac{R_2}{R_1 + R_2}\right) V_{DD} = \left(\frac{1.0M\Omega}{7.8M\Omega}\right) 12V = 1.54V$$

$$V_{GS} = V_G - V_S = 1.54V - 3.34V = -1.8V$$

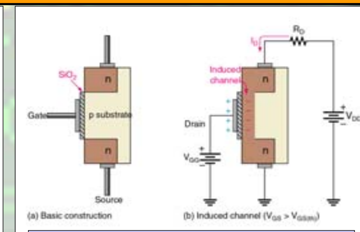
The MOSFET

The metal oxide semiconductor field effect transistor (**MOSFET**) is the second category of FETs. The chief difference is that there no actual pn junction as the p and n materials are insulated from each other. MOSFETs are static sensitive devices and must be handled by appropriate means.

There are depletion MOSFETs (D-MOSFET) and enhancement MOSFETs (E-MOSFET). Note the difference in construction. The E-MOSFET has no structural channel.



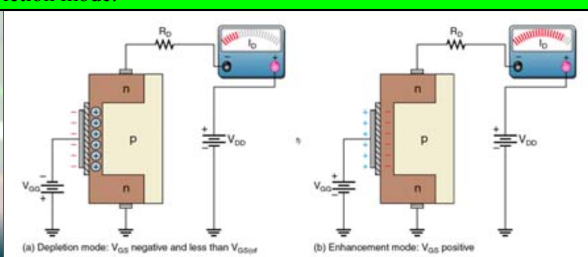
Representation of the basic structure of D-MOSFETs.



Representation of the basic E-MOSFET construction and operation (*n*-channel).

The MOSFET – Depletion MOSFET

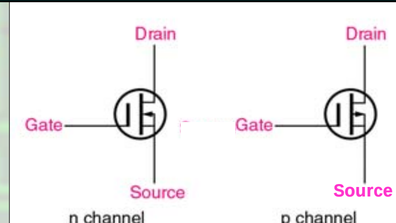
The D-MOSFET can be operated in either of two modes – the depletion mode or enhancement mode – and is sometimes called a depletion/enhancement MOSFET. Since the gate is insulated from the channel, either positive or a negative gate voltage can be applied. The n-channel MOSFET operates in the **depletion** mode when a negative gate-to-source voltage is applied and in the **enhancement** mode when a positive gate-to-source voltage is applied. These devices are generally operated in the depletion mode.



The MOSFET – Depletion MOSFET

Depletion Mode With a negative gate voltage, the negative charges on the gate repel conduction electrons from the channel, leaving positive ions in their place. Thereby, the n channel is depleted of some of its electrons, thus decreasing the channel conductivity. The greater the negative voltage on the gate, the greater the depletion of n-channel electrons. At sufficiently negative gate-to-source voltage, $V_{GS(off)}$, the channel is totally depleted and drain current is zero.

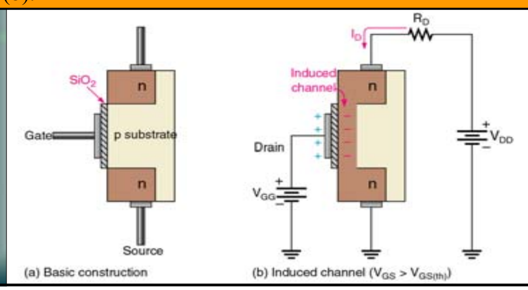
Enhancement Mode With a positive gate voltage, more conduction electrons are attracted into the channel, thus increasing (enhancing) the channel conductivity.



D-MOSFET schematic symbols.

The MOSFET – Enhancement MOSFET (E-MOSFET)

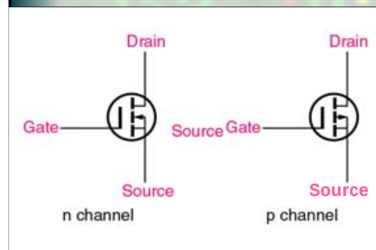
The E-MOSFET operates only in the **enhancement mode** and has no depletion mode. It differs in construction from the D-MOSFET in that it has no structural channel. Notice in Figure (a) that the substrate extends completely to the SiO_2 layer. For n-channel device, a positive gate voltage above threshold value induces a channel by creating a thin layer of negative charges in the substrate region adjacent to the SiO_2 layer, as shown in Figure (b).



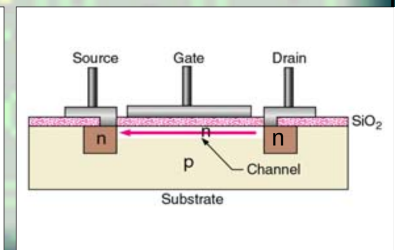
Representation of the basic E-MOSFET construction and operation (*n*-channel).

The MOSFET – Enhancement MOSFET (E-MOSFET)

The schematic symbols for the n-channel and p-channel E-MOSFET are shown in Figure below.

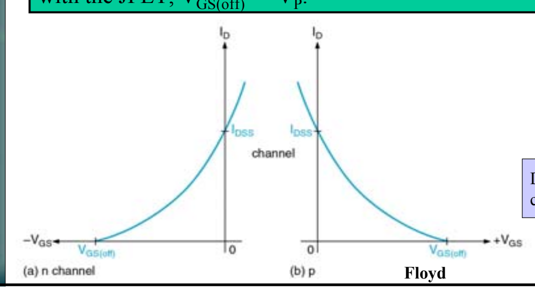


The conventional enhancement MOSFETs have a long thin lateral channel as shown in structural view in Figure below.



MOSFET Characteristics and Parameters – D-MOSFET Transfer Characteristic

As previously discussed, the D-MOSFET can operate with either positive or negative gate voltages. This is indicated on the general transfer characteristic curves in Figure for both n-channel and p-channel MOSFETs. The point on the curves where $V_{GS} = 0$ corresponds to I_{DSS}. The point where $I_D = 0$ corresponds to $V_{GS(off)}$. As with the JFET, $V_{GS(off)} = -V_P$.



D-MOSFET general transfer characteristic curves.

Ex. 7-8 For a certain D-MOSFET, I_{DSS} = 10 mA and $V_{GS(off)}$ = - 8 V.
(a) Is this an n-channel or a p-channel?
(b) Calculate I_D at V_{GS} = - 3 V
(c) Calculate I_D at V_{GS} = + 3 V.

(a) The device has a negative $V_{GS(off)}$; therefore, it is a **n-channel** MOSFET.

$$(b)\quad I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_{GS(off)}}\right)^2 = (10\,mA)\left(1-\frac{-3V}{-8V}\right)^2 = 3.91\,mA$$

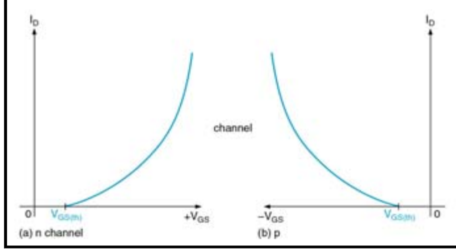
$$(c)\quad I_D = (10\,mA)\left(1-\frac{+3V}{-8V}\right)^2 = 18.9\,mA$$

MOSFET Characteristics and Parameters – E-MOSFET Transfer Characteristic

The E-MOSFET for all practical purposes does not conduct until V_{GS} reaches the threshold voltage ($V_{GS(th)}$). I_D when it is when conducting can be determined by the formulas below. The constant K must first be determined. $I_{D(on)}$ is a data sheet given value.

$$K = I_{D(on)} /(V_{GS} - V_{GS(th)})^2$$

$$I_D = K(V_{GS} - V_{GS(th)})2$$



An n-channel device requires a positive gate-to-source voltage, and a p-channel device requires a negative gate-to-source voltage.

E-MOSFET general transfer characteristic curves.

Ex. 7-9 The data sheet for a 2N7008 E-MOSFET gives $I_{D(on)}$ = 500 mA (minimum) at V_{GS} = 10 V and $V_{GS(th)}$ = 1 V. Determine the drain current for V_{GS} = 5 V.

First, solve for K using Equation,

$$K = \frac{I_{D(on)}}{(V_{GS} - V_{GS(th)})^2} = \frac{500\ mA}{(10V - 1V)^2} = \frac{500\ mA}{81V^2} = 6.17\ mA/V^2$$

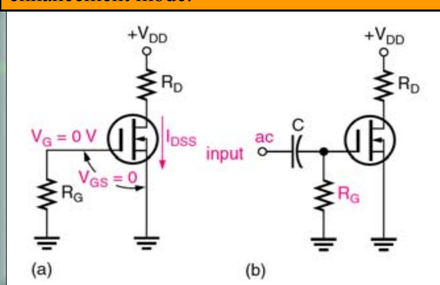
Next, using the value of K, calculate I_D for V_{GS} = 5 V.

$$I_D = K(V_{GS} - V_{GS(th)})^2 = (6.17\ mA/V^2)(5V - 1V)^2 = 98.7\ mA$$

MOSFET Biasing – D-MOSFET Bias

The three ways to bias a MOSFET are zero-bias, voltage-divider bias, and drain-feedback bias.

For D-MOSFET zero biasing as the name implies has no applied bias voltage to the gate. The input voltage swings it into depletion and enhancement mode.



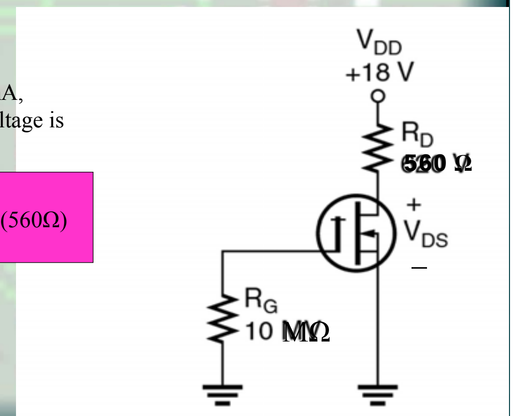
Since V_{GS} = 0, $I_D = I_{DSS}$ as indicated.

$$\mathbf{V_{DS} = V_{DD} - I_{DSS}R_D}$$

Ex. 7-10 Determine the drain-to-source voltage in the circuit of Figure. The MOSFET data sheet gives $V_{GS(off)}$ = - 8 V and I_{DSS} = 12 mA.

Since $I_D = I_{DSS}$ = 12 mA, the drain-to-source voltage is

$V_{DS} = V_{DD} – I_{DSS}R_D$
= 18 V – (12 mA)(560Ω)
= 11.28 V



EET1240/ET212 Electronics

Amplifier Frequency Response

Electrical and Telecommunications
Engineering Technology Department

Professor Jang

Prepared by textbook based on "Electronics Devices"
by Floyd, Prentice Hall, 7th edition.

Outlines

- Introduction to Frequency Response of an Amplifier
- Gain of an Amplifier in Decibels (dB)
- Frequency Response of a BJT Amplifier
- Frequency Response of an FET Amplifier
- Frequency Response of a Multistage Amplifier

Key Words: Frequency Response, Amplifier, Decibel, BJT, FET, Multistage

Amplifier Frequency Response - Introduction

Most amplifiers have a finite range of frequencies in which it will operate. We will discuss what determines the frequency response of an amplifier circuit and how it is measured.

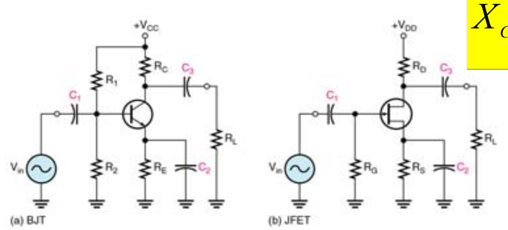
Basic Concepts

When frequency is low enough, the coupling and bypass capacitors can no longer be considered as shorts because their reactances are large enough to have significant effect. Also, when the frequency is high enough, the internal transistor capacitances can no longer be considered as opens because their reactances become small enough to have significant effect on the amplifier operation. We will discuss how the capacitor limits the passage of certain frequencies. This is called the **frequency response** of an amplifier.

Basic Concepts – Effect of Coupling Capacitors

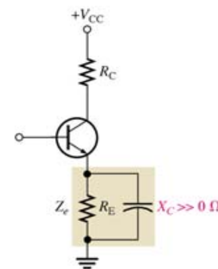
Coupling capacitors C_1 and C_3 limit the passage of very low frequencies. Emitter bypass C_2 capacitor will have high reactance to low frequencies as well, limiting the gain. Also the capacitance causes a phase shift of the signal.

$$X_C = \frac{1}{2\pi f C}$$



Basic Concepts – Effect of Bypass Capacitors

At lower frequencies, the reactance of the emitter bypass capacitor, C_2 in previous Figure, becomes significant and emitter is no longer at ac ground. The capacitive reactance X_{C_2} in parallel with R_E creates an impedance that reduces the gain as shown in Figure.



Nonzero reactance of the bypass capacitor in parallel with R_E creates an emitter impedance, (Z_e), which reduces the voltage gain.

When the frequency is sufficiently high $X_C \approx 0\ \Omega$ and the voltage gain of the CE amplifier is

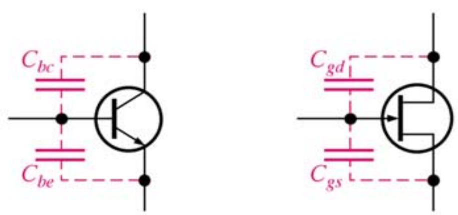
$$A_v = \frac{R_C}{r'_e}$$

At lower frequencies, $X_C >> 0\ \Omega$ and the voltage gain is

$$A_v = \frac{R_C}{(r'_e + Z_e)}$$

Basic Concepts – Effect of Internal Transistor Capacitances

At high frequencies, the coupling and bypass capacitors become effective ac shorts and do not affect an amplifier's response. Internal transistor junction capacitances, however, do come into play, reducing an amplifier's gain and introducing phase shift as the signal frequency increases.

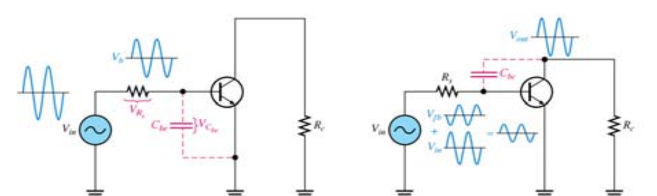


(a) BJT (b) JFET

C_{be} is the base-emitter junction capacitance and C_{bc} is the base-collector junction capacitance.

Basic Concepts – Effect of Internal Transistor Capacitances

When the reactance of C_{be} becomes small enough, a significant amount of the signal voltage is lost due to a voltage-divider effect of the signal source resistance and the reactance of C_{be} as illustrated in Figure (a). When the resistance of C_{bc} becomes small enough, a significant amount of output signal voltage is fed back out of phase with input (negative feedback), thus effectively reducing the voltage gain as shown in Figure (b).

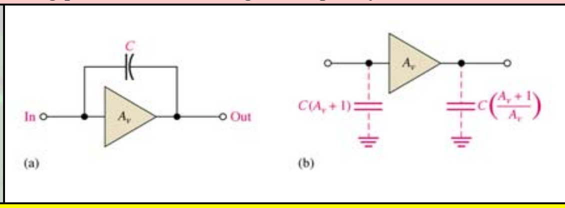


(a) Effect of C_{be}, where V_b is reduced by the voltage-divider action of R_s and $X_{C_{be}}$.

(b) Effect of C_{bc}, where part of V_{out} (V_{fb}) goes back through C_{bc} to the base and reduces the input signal because it is approximately 180° out of phase with V_{in}.

Basic Concepts – Miller's Theorem

At high frequencies, the coupling and bypass capacitors become effective ac shorts and do not affect an amplifier's response. Internal transistor junction capacitances, however, do come into play, reducing an amplifier's gain and introducing phase shift as the signal frequency increases.

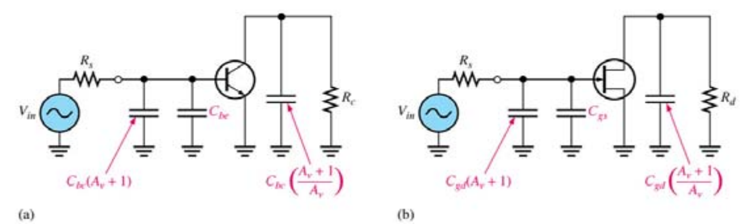


Miller's theorem states that C effectively appears as a capacitance from input and output to ground, as shown in Figure (b).

$$C_{in(Miller)} = C(A_v + 1) \qquad C_{out(Miller)} = C\left(\frac{A_v + 1}{A_v}\right)$$

Basic Concepts – Miller's Theorem

Millers theorem allows us to view the internal capacitances as external capacitors for better understanding of the effect they have on the frequency response.



The Decibel

The **decibel** is a common unit of measurement of voltage gain and frequency response. It is a logarithmic measurement of the ratio of one power to another or one voltage to another. The formulas below are used for calculation of decibels for power gain and voltage gain.

$$A_{p(db)} = 10 \log A_p$$

$$A_{v(db)} = 20 \log A_v$$

Table shows how doubling or having voltage gains translates into dB values. Notice in the table that every time the voltage gain is doubled, the dB value increases by 6 dB, and every time the gain is halved, the dB value decreases by 6 dB.

VOLTAGE GAIN (A_v)	dB (WITH RESPECT TO ZERO REFERENCE)
32	20 log(32) = 30 dB
16	20 log(16) = 24 dB
8	20 log(8) = 18 dB
4	20 log(4) = 12 dB
2	20 log(2) = 6 dB
1	20 log(1) = 0 dB
0.707	20 log(0.707) = - 3 dB
0.5	20 log(0.5) = - 6 dB
0.25	20 log(0.25) = - 12 dB
0.125	20 log(0.125) = - 18 dB
0.0625	20 log(0.0625) = - 24 dB
0.03125	20 log(0.03125) = - 30 dB

Ex 10-1 Express each of the following ratios in dB:

(a) $\frac{P_{out}}{P_{in}} = 250$ (b) $\frac{P_{out}}{P_{in}} = 100$ (c) $A_v = 10$

(d) $A_p = 0.5$ (e) $\frac{V_{out}}{V_{in}} = 0.707$

(a) $A_{p(dB)} = 10 \log(250) = 24$ dB (b) $A_{p(dB)} = 10 \log(100) = 20$ dB

(c) $A_{v(dB)} = 20 \log(10) = 20$ dB (d) $A_{p(dB)} = 10 \log(0.5) = -3$ dB

(e) $A_{v(dB)} = 20 \log(0.707) = -3$ dB

The Decibel – The Critical Frequency

The **critical frequency** also known as the **cutoff frequency** is the frequency at which the output power drops by 3 dB, which represents one-half of it's midrange value. An output voltage drop of 3 dB represents about a 70.7% drop from the midrange value.

Power is often measured in units of **dBm**. This is decibels with reference to 1mW of power. This means that 0 dBm = 1mW.

Ex 10-2 A certain amplifier has a midrange rms output voltage of 10 V. What is the rms output voltage for each of the following dB gain reductions with a constant rms input voltage?
(a) – 3 dB (b) – 6 dB (c) – 12 dB (d) – 24 dB

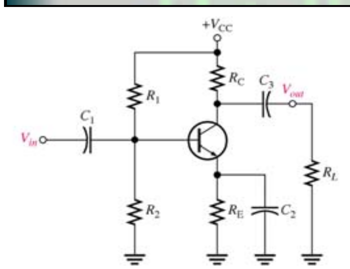
Multiply the midrange output voltage by the voltage gain corresponding to the specified dB value in Table.

(a) At – 3 dB, $V_{out} = 0.707(10\text{ V}) = 7.07$ V
(b) At – 6 dB, $V_{out} = 0.5(10\text{ V}) = 5$ V
(c) At – 12 dB, $V_{out} = 0.25(10\text{ V}) = 2.5$ V
(d) At – 24 dB, $V_{out} = 0.0625(10\text{ V}) = 0.625$ V

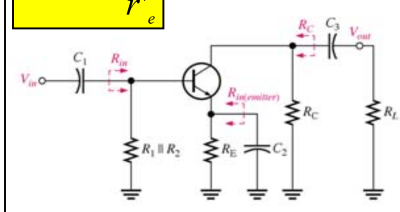
Low-Frequency Amplifier Response

In looking at the low frequency ac equivalent circuit of a capacitor coupled amplifier we can see there are three RC circuits which will limit low frequency response. The input at the base, the output at the collector, and the emitter.

$$A_{v(mid)} = \frac{R_c}{r'_e}$$



A capacitively coupled amplifier.



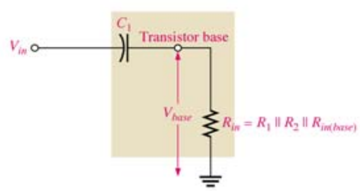
The low-frequency ac equivalent circuit of the amplifier in Figure (left) consists of three high-pass RC circuits.

Low-Frequency Amplifier Response – The Input RC Circuit

The input RC circuit for the BJT amplifier is formed by C_1 and the amplifier's input resistance and is shown in Figure.

$$V_{base} = \left(\frac{R_{in}}{\sqrt{R_{in}^2 + X_{C_1}^2}} \right) V_{in}$$

The input circuits effects on the signal at a given frequency can be more easily understood by looking at this simplified input circuit. The frequency at which the gain is down by 3dB is called the **lower critical frequency (f_c)**. This frequency can be determined by the formula below.



Input RC circuit formed by the input coupling capacitor and the amplifier's input resistance.

$$X_{C1} = \frac{1}{2\pi f_c C_1} = R_{in} \qquad f_c = \frac{1}{2\pi R_{in} C_1} \qquad f_c = \frac{1}{2\pi (R_s + R_{in}) C_1}$$

Ex 10-3 For an input RC circuit in a certain amplifier, R_{in} = 1.0 kΩ and C_1 = 1 μF. Neglect the source resistance.
(a) Determine the lower critical frequency.
(b) What is the attenuation of the input RC circuit at the lower critical frequency?
(c) If the midrange voltage gain of the amplifier is 100, what is the gain at the lower critical frequency?

(a) $$f_c = \frac{1}{2\pi R_{in} C_1} = \frac{1}{2\pi (1.0k\Omega)(1\mu F)} = 159 Hz$$

(b) At f_c, $X_{c1} = R_{in}$. Therefore

$$Attenuation = \frac{V_{base}}{V_{in}} = 0.707$$

(c) $A_v = 0.707\, A_{v(mid)} = 0.707(100) = 70.7$

Low-Frequency Amplifier Response – Voltage gain roll-off at low frequency

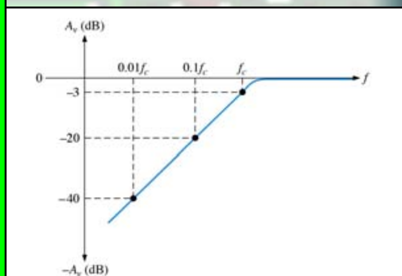
The decrease in voltage gain with frequency is called **roll-off**. Let's take a frequency that is one-tenth of the critical frequency ($f = 0.1 f_c$). Since $X_{c1} = R_{in}$ at f_c, then $X_{c1} = 10\,R_{in}$ at $0.1 f_c$ because of the inverse relationship of X_{C1} and f_c. The attenuation of the input RC circuit is, therefore,

$$\text{Attenuation} = \frac{V_{base}}{V_{in}} = \frac{R_{in}}{\sqrt{R_{in}^2 + X_{C1}^2}} = \frac{R_{in}}{\sqrt{R_{in}^2 + (10R_{in})^2}}$$
$$= \frac{R_{in}}{\sqrt{R_{in}^2 + 100R_{in}^2}} = \frac{R_{in}}{\sqrt{R_{in}^2(1+100)}}$$
$$= \frac{R_{in}}{R_{in}\sqrt{101}} = \frac{1}{\sqrt{101}} \cong \frac{1}{10} = 0.1$$

The dB attenuation is $$20\log\left(\frac{V_{base}}{V_{in}}\right) = 20\log(0.1) = -20dB$$

Low-Frequency Amplifier Response – dB/decade

The decrease in voltage gain with frequency is called the **roll-off**. A ten times change in frequency is called a **decade**. The attenuation measured in dB at each decade is is the **dB/decade**. This typical dB A_v vs frequency illustrates the relationship. Sometimes roll-off is expressed in **dB/octave**, which is a doubling or halving of a the frequency.



dB voltage gain versus frequency for the input RC circuit.

Ex 10-4 The midrange voltage gain if a certain amplifier is 100. The input RC circuit has a lower critical frequency of 1 kHz. Determine the actual voltage gain at f = 1 kHz, f = 100 Hz, and f = 10 Hz.

When f = 1 kHz, the voltage gain is 3 dB less than at midrange. At – 3 dB, the voltage gain is reduced by a factor of 0.707.

$$A_v = (0.707)(100) = 70.7$$

When f = 100 Hz = 0.1f_c, the voltage gain is 20 dB less than at f_c. The voltage gain at – 20 dB is one-tenth of that at the midrange frequencies.

$$A_v = (0.1)(100) = 10$$

When f = 10 Hz = 0.01fc, the voltage gain is 20 dB less than at f = 0.1f_c or – 40 dB. The voltage gain at – 40 dB is one-tenth of that at – 20 dB or one--hundredth that at the midrange frequencies.

$$A_v = (0.01)(100) = 1$$

Low-Frequency Amplifier Response – Phase shift in the input RC circuit

In addition to reducing the voltage gain, the input RC circuit also causes an increasing phase shift through an amplifier as the frequency decreases.

$$\theta = \tan^{-1}\left(\frac{X_{C1}}{R_{in}}\right)$$

For midrange frequencies, $X_{c1} \approx 0\ \Omega$, so

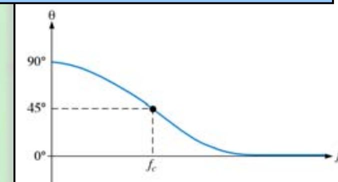
$$\theta = \tan^{-1}\left(\frac{0\Omega}{R_{in}}\right) = \tan^{-1}(0) = 0^o$$

At the critical frequency, $X_{c1} = R_{in}$, so

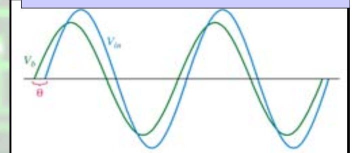
$$\theta = \tan^{-1}\left(\frac{R_{in}}{R_{in}}\right) = \tan^{-1}(1) = 45^o$$

A decade below the critical frequency, $X_{c1} = 10R_{in}$, so

$$\theta = \tan^{-1}\left(\frac{10R_{in}}{R_{in}}\right) = \tan^{-1}(10) = 84.3^o$$



Phase angle versus frequency for the input RC circuit.

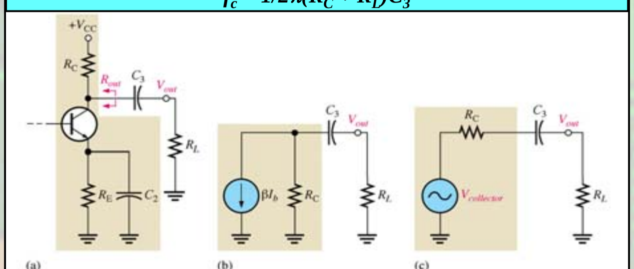


Input RC circuit causes the base voltage to lead the input voltage below midrange by an amount equal to the circuit phase angle.

Low-Frequency Amplifier Response – The Output RC Circuit

The output RC circuit affects the response similarly to the input RC circuit. The formula below is used to determine the cutoff frequency of the output circuit.

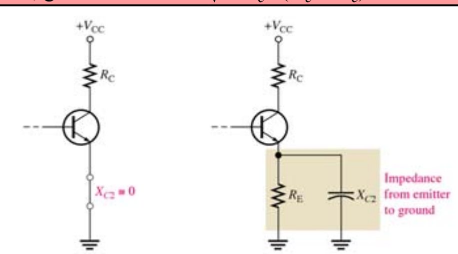
$$f_c = 1/2\pi(R_C + R_L)C_3$$



Development of the equivalent low-frequency output RC circuit.

Low-Frequency Amplifier Response- The Bypass RC Circuit

The bypass RC circuit is no different in it's effect on the gain at low frequencies. For midrange frequencies it is assumed that $X_{C2} \approx 0\ \Omega$, effectively shorting the emitter to ground so that the amplifier gain is R_c/r'_e. As frequency is reduced, X_{C2} increases. The impedance from emitter to ground increases, gain decreases. $A_v = R_c / (r'_e + R_e)$

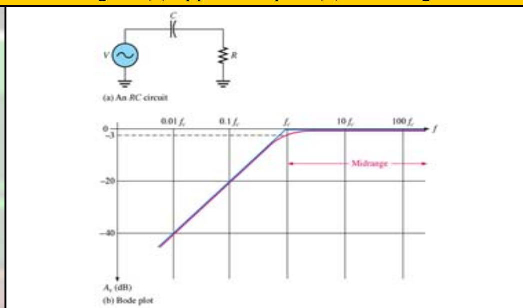


(a) For midrange frequencies, C_2 effectively shorts the emitter to ground.

(b) Below f_c, X_{C2} and R_E form an impedance between the emitter and ground.

Low-Frequency Amplifier Response- The Bode Plot

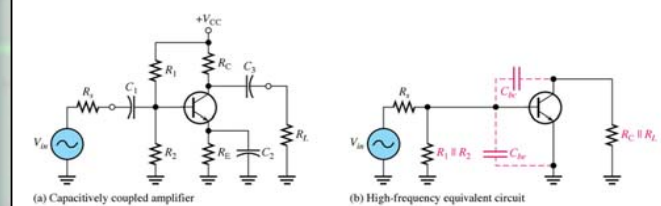
A plot of dB voltage gain versus frequency on semilog paper (logarithmic horizontal axis scale and a linear vertical axis scale) is called a **Bode plot**. A generalized Bode plot for an RC circuit like that shown in Figure (a) appears in part (b) of the figure.



An RC circuit and its low-frequency response. (Blue is ideal; red is actual.)

High-Frequency Amplifier Response

A high-frequency ac equivalent circuit for the BJT amplifier in Figure. Notice that the coupling and bypass capacitors are treated as effective shorts and do not appear in the equivalent circuit. The internal capacitances, C_{be} and C_{bc}, which are significant only at high frequencies, do appear in the diagram.



Capacitively coupled amplifier and its high-frequency equivalent circuit.

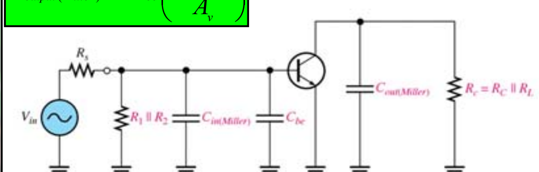
High-Frequency Amplifier Response – Miller's Theorem in High-Frequency Analysis

Looking in from the signal source, the capacitance C_{bc} appears in the Miller input capacitance from base to ground.

$$C_{in(Miller)} = C_{bc}(A_v + 1)$$

C_{be} simply appears as a capacitance to ac ground, as shown in Figure, in parallel with $C_{in(Miller)}$. Looking in at collector, C_{bc} appears in the Miller output capacitance from collector to ground. As shown in Figure.

$$C_{output(Miller)} = C_{bc}\left(\frac{A_v + 1}{A_v}\right)$$

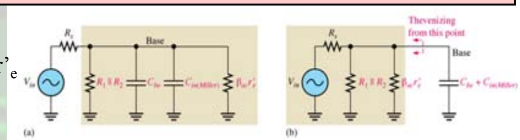


High-frequency equivalent circuit after applying Miller's theorem.

Low-Frequency Amplifier Response- The Input RC Circuit

At high frequencies, the input circuit is as shown in Figure (a), where $\beta_{ac} r'_e$ is the input resistance. By combining C_{be} and $C_{in(Miller)}$ in parallel and repositioning shown in Figure (b). By thevenizing the circuit to left of capacitor, as indicated, the input RC circuit is reduced to the equivalent form shown in Figure (c).

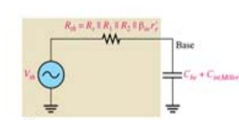
$X_{Ctot} = R_s||R_1||R_2||\beta_{ac} r'_e$



Therefore,

$1/(2\pi f_c C_{tot}) = R_s||R_1||R_2||\beta_{ac}r'_e$

and



$f_c = 1/(2\pi(Rs||R1||R2||\beta_{ac}r'_e)C_{tot}$

Where R_s is the resistance of the signal source and $C_{tot} = C_{be} + C_{in(miller)}$.

Ex 10-10 Derive the input RC circuit for the BJT amplifier in Figure. Also determine the critical frequency. The transistor's data sheet provides the following: β_{ac} = 125, C_{be} = 20 pF, and C_{bc} = 2.4 pF.

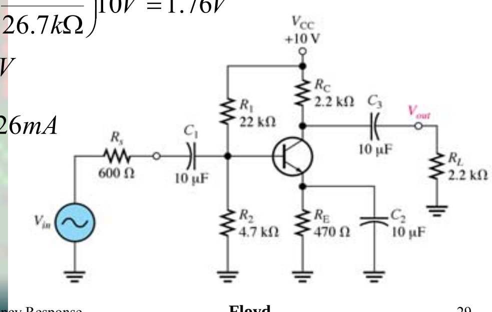
First, find r'_e as follows:

$$V_B = \left(\frac{R_2}{R_1 + R_2}\right)V_{CC} = \left(\frac{4.7k\Omega}{26.7k\Omega}\right)10V = 1.76V$$

$$V_E = V_B - 0.7V = 1.06V$$

$$I_E = \frac{V_E}{R_E} = \frac{1.06V}{470\Omega} = 2.26mA$$

$$r'_e = \frac{25mV}{I_E} = 11.1\Omega$$



The total resistance of the input circuit is

$R_{in(tot)} = R_s \| R_1 \| R_2 \| \beta_{ac} r'_e$ = 600 Ω‖22 kΩ‖4.7 kΩ‖125(11.1 Ω) = 378 Ω

Next, in order to determine the capacitance, you must calculate the midrange gain of the amplifier so that you can apply Miller's theorem.

$$A_{v(mid)} = \frac{R_c}{r'_e} = \frac{R_C // R_L}{r'_e} = \frac{1.1k\Omega}{11.1\Omega} = 99$$

Apply Miller's theorem.

$C_{in(Miller)} = C_{bc}(A_{v(mid)} + 1)$ = (2.4 pF)(100) = 240 pF

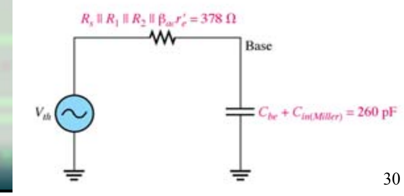
The total input capacitance is $C_{in(Miller)}$ in parallel with C_{be}.

$C_{in(tot)} = C_{in(Miller)} + C_{be}$ = 240 pF + 20 pF = 260 pF

$$f_c = \frac{1}{2\pi(R_{in(tot)})(C_{in(tot)})}$$

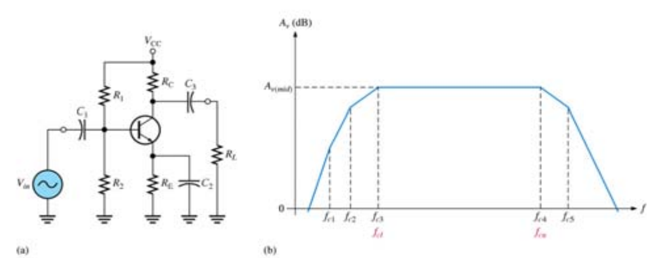
$$= \frac{1}{2\pi(378\Omega)(260pF)}$$

$$= 1.62MHz$$



Total Amplifier Frequency Response

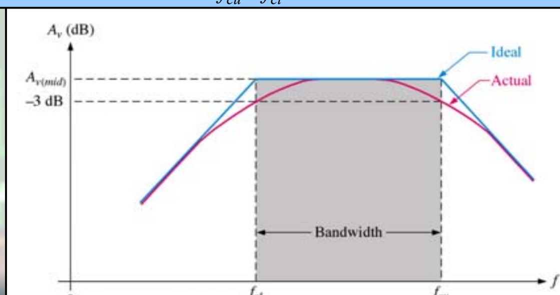
Figure (b) shows a generalized ideal response curve (Bode plot) for the BJT amplifier shown in Figure (a). The three break points at the lower critical frequencies (f_{c1}, f_{c2}, and f_{c3}) are produced by the three low-frequency RC circuits formed by the coupling and bypass capacitors. The break points at the upper critical frequencies, f_{c4} and f_{c5}, are produced by the two high-frequency RC circuit formed by the transistor's internal capacitances.



Total Amplifier Frequency Response - Bandwidth

An amplifier normally operates with signal frequencies between f_{cl} and f_{cu}. The range (band) of frequencies lying between f_{cl} and f_{cu} is defined as the **bandwidth** of the amplifier, as illustrated in Figure. The amplifier's bandwidth is expressed in units of hertz as

$$BW = f_{cu} - f_{cl}$$



EET1240/ET212 Electronics

Operational Amplifier

Electrical and Telecommunications Engineering Technology Department

Professor Jang

Prepared by textbook based on "Electronics Devices" by Floyd, Prentice Hall, 7th edition.

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Sunghoon Jang

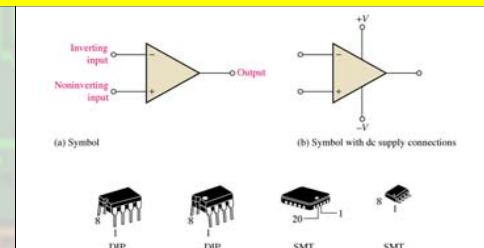
Outlines

- Introduction to operational amplifier (OP-Amp)
- The Parameters and Characteristics of an Op-Amp.
- Basic Op-Amp Operation
- Three Op-Amp Configurations and Closed-loop Frequency Response of an Op-Amp.

Key Words: Operational Amplifier, CMRR, Inverting, Noninverting, Open Loop Gain

Introduction To Operational Amplifiers

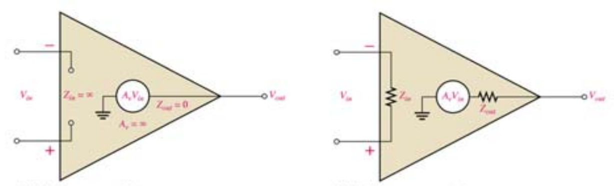
The **operational amplifier** or op-amp is a circuit of components integrated into one chip. We will study the op-amp as a singular device. A typical op-amp is powered by two dc voltages and has an inverting(-) and a noninverting input (+) and an output. Note that for simplicity the power terminals are not shown but understood to exist.



(c) Typical packages. Pin 1 is indicated by a notch or dot on dual-in-line (DIP) and surface-mount technology (SMT) packages, as shown.

Introduction To Op-Amps – The Ideal & Practical Op-Amp

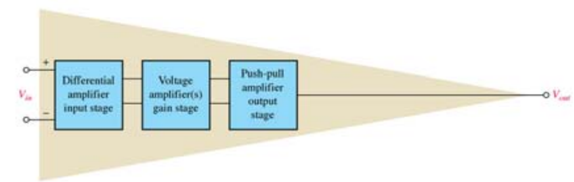
While an **ideal op-amp** has infinite voltage gain and infinite bandwidth. Also, it has infinite input impedance (open) and zero output impedance. We know this is impossible. However, **Practical op-amps** do have very high voltage gain, very high input impedance, very low output impedance, and wide bandwidth.



(a) Ideal op-amp representation (b) Practical op-amp representation

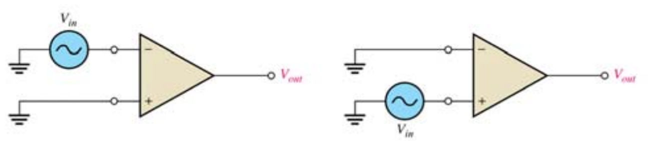
Introduction To Op-Amps – Internal Block Diagram of an Op-Amp

A typical op-amp is made up of three types of amplifier circuit: a *differential amplifier*, a *voltage amplifier*, and a *push-pull amplifier*, as shown in Figure. A differential amplifier is the input stage for the op-amp. It has two inputs and provides amplification of the difference voltage between the two inputs. The voltage amplifier provides additional op-amp gain. Some op-amps may have more than one voltage amplifier stage.



Op-Amp Input Modes and Parameters – Input Signal Modes – Signal-Ended Input

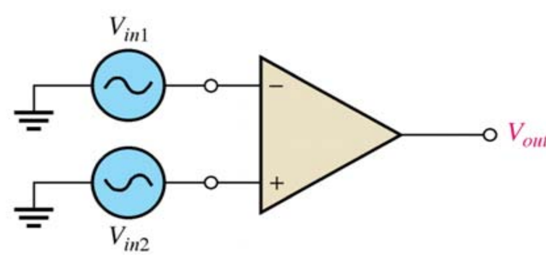
When an op-amp is operated in the **single-ended mode**, one input is grounded and signal voltage is applied only to the other input as shown in Figure. In the case where the signal voltage is applied to the *inverting input* as in part (a), an inverted, amplified signal voltage appears at the output. In the case where the signal voltage is applied to the *noninverting input* with the inverting input grounded, as in part (b), a noninverted, amplified signal voltage appears at the output.



(a) (b)

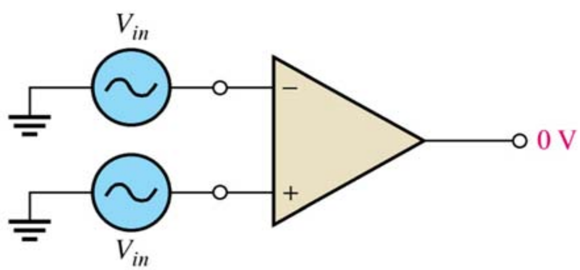
Op-Amp Input Modes and Parameters – Input Signal Modes - Differential Input

In the **differential mode**, two opposite-polarity (out-of-phase) signals are applied to the inputs, as shown in Figure. This type of operation is also referred to as double-ended. The amplified difference between the two inputs appears on the output.

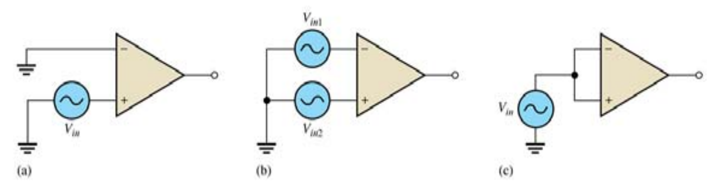


Op-Amp Input Modes and Parameters – Input Signal Modes - Common-Mode Input

In the common mode, two signal voltages of the same phase, frequency, and amplitude are applied to the two inputs, as shown in Figure. When equal input signals are applied to both inputs, they cancel, resulting in a zero output voltage. This action is called common-mode rejection.



Ex. 12-1 Identify the type of input mode for each op-amp in Figure.



(a) Single-ended input **(b)** Differential input **(c)** Common-mode

Op-Amp Input Modes and Parameters – Common-Mode Rejection Ratio

The **common-mode rejection ratio (CMRR)** is the measure for how well it rejects an unwanted the signal. It is the ratio of open loop gain (A_{ol}) to common-mode gain (A_{cm}). The open loop gain is a data sheet value.

$$CMRR = \frac{A_{ol}}{A_{cm}}$$

The CMRR is often expressed in decibel (dB) as

$$CMRR = 20\log\left(\frac{A_{ol}}{A_{cm}}\right)$$

Ex. 12-2 A certain op-amp has an open-loop voltage gain of 100,000 and a common-mode gain of 0.2. Determine the CMRR and express it in decibel.

A_{ol} = 100,000, and A_{cm} = 0.2. Therefore,

$$CMRR = \frac{A_{ol}}{A_{cm}} = \frac{100{,}000}{0.2} = 500{,}000$$

Expressed in decibels,

$$CMRR = 20\log(500{,}000) = 114dB$$

Ex. 12-3 An op-amp data sheet specifies a CMRR of 300,000 and an A_{ol} of 90,000. What is the common-mode gain?

$$A_{cm} = \frac{A_{ol}}{CMRR} = \frac{90{,}000}{300{,}000} = 0.3$$

Op-Amp Input Modes and Parameters

Op-amps tend to produce a small dc voltage called output error voltage ($V_{OUT(error)}$). The data sheet provides the value of dc differential voltage needed to force the output to exactly zero volts. This is called the **input offset voltage** (**V_{OS}**). This can change with temperature and the **input offset drift** is a parameter given on the data sheet.

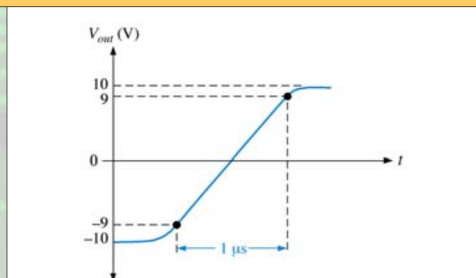
Op-Amp Input Modes and Parameters

There are other input parameters to be considered for op-amp operation. The **input bias current** is the dc current required to properly operate the first stage within the op-amp. The **input impedance** is another. Also, the **input offset current** which can become a problem if both dc input currents are not the same.

Output impedance and **slew rate**, which is the response time of the output with a given pulse input are two other parameters.

Op-amp low **frequency response** is all the way down to dc. The high frequency response is limited by the internal capacitances within the op-amp stages.

Ex. 12-4 The output voltage of a certain op-amp appears as shown in Figure in response to a step input. Determine the slew rate.

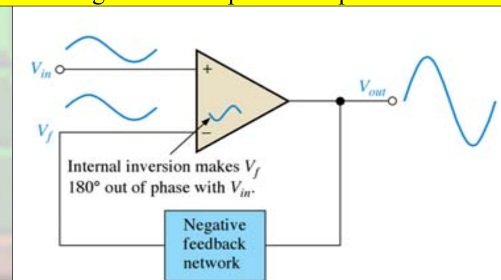


The output goes from the lower to the upper limit in 1 μs. Since this response is not ideal, the limits are taken at the 90% points, as indicated. So, the upper limit is +9 V and the lower limit is -9 V. The slew rate is

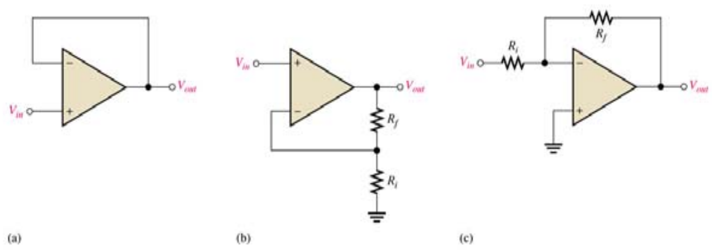
$$Slew\ rate = \frac{\Delta V_{out}}{\Delta t} = \frac{+9V-(-9V)}{1\,\mu s} = 18\,V/\mu s$$

Negative Feedback

Negative feedback is feeding part of the output back to the input to limit the overall gain. This is used to make the gain more realistic so that the op-amp is not driven into saturation. Remember regardless of gain there are limitations of the amount of voltage that an amplifier can produce.



Ex. 12-5 Identify each of the op-amp configurations in Figure.



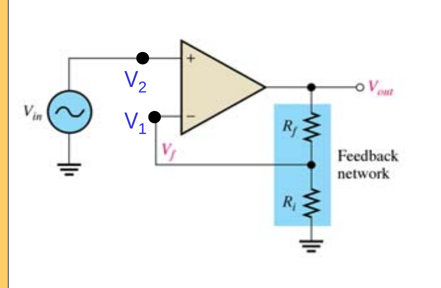
(a) Voltage-follower **(b)** Non-inverting **(c)** Inverting

Op-Amps With Negative Feedback – noninverting Amplifier

The **closed-loop voltage gain (A_{cl})** is the voltage gain of an op-amp with external feedback. The gain can be controlled by external component values. Closed loop gain for a **non-inverting amplifier** can be determined by the formula below.

Ideal Op-Amp

$V_1 = V_2 = V_{in}$



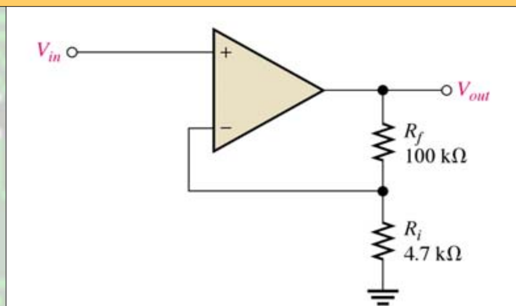
$$\frac{V_1}{R_i} + \frac{V_1 - V_{out}}{R_f} = 0$$

$$V_{in} \cdot R_f + R_i(V_{in} - V_{out}) = 0$$

$$V_{in}(R_i + R_f) = R_i \cdot V_{out}$$

$$V_{out} = \frac{R_i + R_f}{R} \cdot V_{in} = (1 + \frac{R_f}{R_i}) \cdot V_{in}$$

Ex. 12-6 Determine the gain of the amplifier in Figure. The open-loop voltage gain of the op-amp is 100,000.

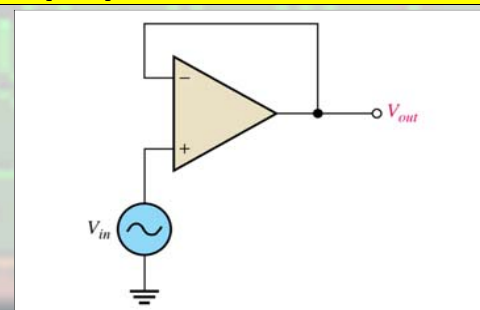


This is a noninverting op-amp configuration. Therefore, the closed-loop voltage gain is

$$A_{cl(NI)} = 1 + \frac{R_f}{R_i} = 1 + \frac{100\,k\Omega}{4.7\,k\Omega} = 22.3$$

Op-Amps With Negative Feedback – Voltage-follower

The **voltage-follower amplifier** configuration has all of the output signal fed back to the inverting input. The voltage gain is **1**. This makes it useful as a buffer amp since it has a high input impedance and low output impedance.

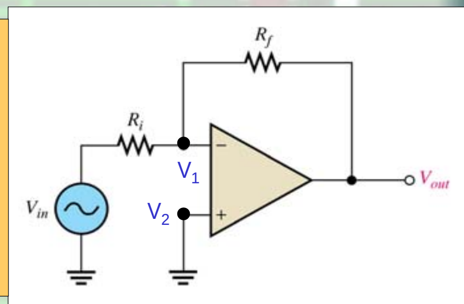


Op-Amps With Negative Feedback – Inverting Amplifier

The **inverting amplifier** has the output fed back to the inverting input for gain control. The gain for the inverting op-amp can be determined by the formula below.

Ideal Op-Amp

$V_1 = V_2 = 0$

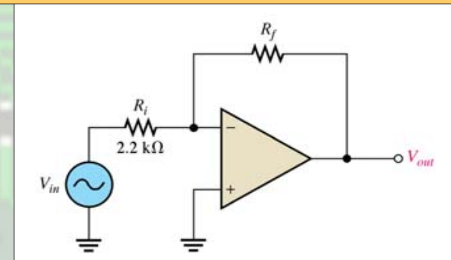


$$\frac{V_1 - V_{in}}{R_i} + \frac{V_1 - V_{out}}{R_f} = 0$$

$$-V_{in}R_f - V_{out}R_i = 0$$

$$V_{out} = -\left(\frac{R_f}{R_i}\right)V_{in}$$

Ex. 12-7 Given the op-amp configuration in Figure, determine the value of R_f required to produce a closed-loop voltage gain of -100.

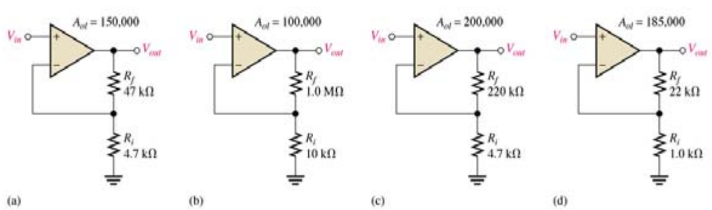


Knowing that R_i = 2.2 kΩ and the absolute value of the closed-loop gain is $|A_{cl(I)}|$ = 100, calculate R_f as follows:

$$|A_{cl(I)}| = \frac{R_f}{R_i}$$

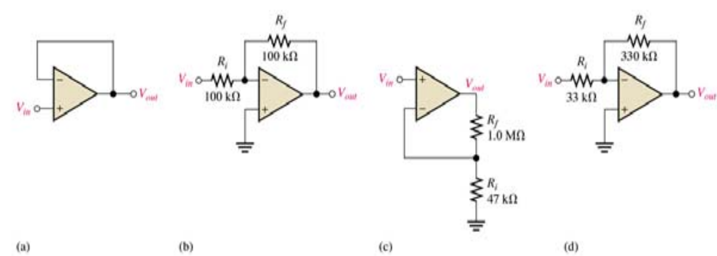
$$R_f = |A_{cl(I)}|R_i = (100)(2.2k\Omega) = 220k\Omega$$

Ex. 12-8 Determine the closed-loop gain of each amplifier in Figure.



(a) 11 **(b)** 101 **(c)** 47.8 **(d)** 23

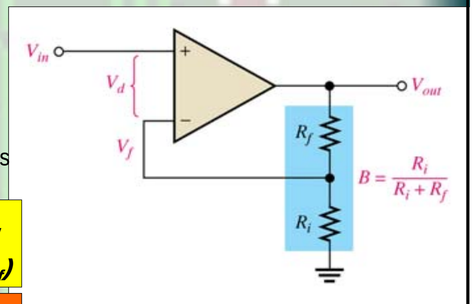
Ex. 12-9 If a signal voltage of 10 mV_{rms} is applied to each amplifier in Figure, what are the output voltages and what is there phase relationship with inputs?.



(a) $V_{out} \cong V_{in}$ = 10 mV, in phase **(b)** $V_{out} = A_{cl}V_{in}$ = – 10 mV, 180º out of phase **(c)** V_{out} = 233 mV, in phase **(d)** V_{out} = – 100 mV, 180º out of phase

Effects Of Negative Feedback On Op-Amp Impedances - Impedances of a Noninverting Amplifier – Input Impedance

However high the input impedance of an op-amp circuit is, impedance still exists. For a non-inverting amplifier it can be determined by the formulas below.



$B_{(feedback\ attenuation)} = 1/A_{cl}$

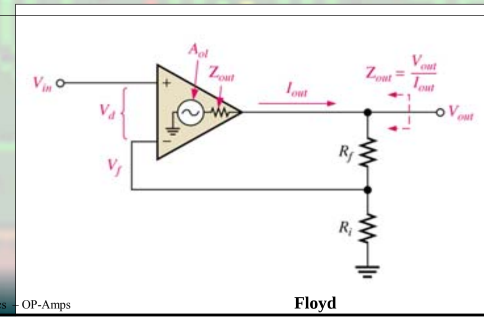
$= R_i/(R_i + R_f)$

$Z_{in(NI)} = (1 + A_{ol}B)Z_{in}$

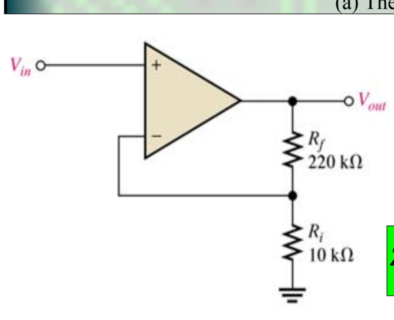
Effects Of Negative Feedback On Op-Amp Impedances - Impedances of a Noninverting Amplifier – Output Impedance

The output impedance is understood to be low for an op-amp. Its exact value can be determined by the formula below.

$Z_{out(NI)} = Z_{out}/(1 + A_{ol}B)$



Ex. 12-10 (a) Determine the input and output impedances of the amplifier in Figure. The op-amp data sheet gives Z_{in} = 2 MΩ, Z_{out} = 75 Ω, and A_{ol} = 200,000. (b) Find the closed-loop voltage gain.



(a) The attenuation, B, of the feedback circuit is

$$B = \frac{R_i}{R_i + R_f} = \frac{10k\Omega}{230k\Omega} = 0.0435$$

$$Z_{in(NI)} = (1 + A_{ol}B)Z_{in} = [1 + (200{,}000)(0.0435)](2M\Omega) = (1 + 8700)(2M\Omega) = 17.4G\Omega$$

$$Z_{out(NI)} = \frac{Z_{out}}{1 + A_{ol}B} = \frac{75\Omega}{1 + 8700} = 8.6m\Omega$$

(b)

$$A_{cl(NI)} = \frac{1}{B} = \frac{1}{0.0435} \cong 23.0$$

Ex. 12-11 The same op-amp in Example 6-10 is used in a voltage-follower configuration. Determine the input and output impedance.

$$\text{Since } B = 1,$$

$$Z_{in(VF)} = (1 + A_{ol})Z_{in} = (1 + 200{,}000)(2\,M\Omega) \cong 400\ G\Omega$$

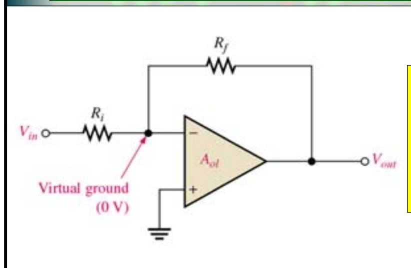
$$Z_{out(VF)} = \frac{Z_{out}}{1 + A_{ol}} = \frac{75\Omega}{1 + 200{,}000} = 375\ \mu\Omega$$

Notice that $Z_{in(VF)}$ is much greater than $Z_{in(NI)}$, and $Z_{out(VF)}$ is much less than $Z_{out(NI)}$ from Example 6-10.

Effects Of Negative Feedback On Op-Amp Impedances – Impedances of an Inverting Amplifier

The input impedance for an inverting amplifier is approximately equal to the input resistor (R_i).

The output impedance is very low and in most cases any impedance load can be connected to it with no problem. The exact amount can be determined by the formulas below.



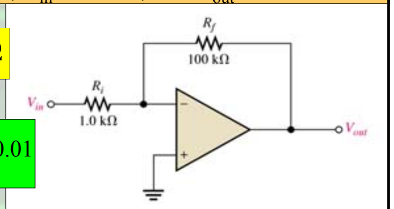
$B_{(feedback\ attenuation)} = R_i/(R_i + R_f)$

$Z_{in(I)} \approx R_i$

$Z_{out(I)} = Z_{out} / (1 + A_{ol}B)$

Ex. 12-12 Find the value of the input and output impedances in Figure. Also, determine the closed-loop voltage gain. The op-amp has the following parameters: A_{ol} = 50,000; Z_{in} = 4 MΩ; and Z_{out} = 50 Ω.

$$Z_{in(I)} \cong R_i = 1.0\ k\Omega$$



The feedback attenuation, B, is

$$B = \frac{R_i}{R_i + R_f} = \frac{1.0\ k\Omega}{101\ k\Omega} \cong 0.01$$

Then

$$Z_{out(I)} = \frac{Z_{out}}{1 + A_{ol}B} = \frac{50\Omega}{1 + (50{,}000)(0.01)} = 99\ m\Omega$$

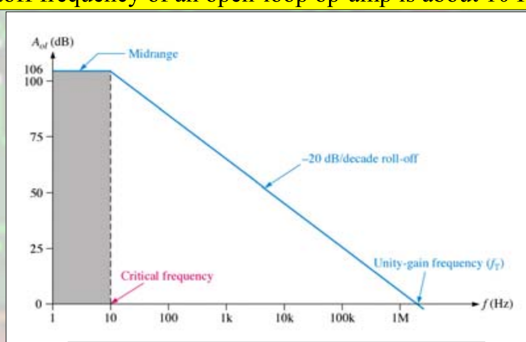
(zero for all practical purposes)

The closed-loop voltage gain is

$$A_{cl(I)} = -\frac{R_f}{R_i} = -\frac{100\ k\Omega}{1.0\ k\Omega} = -100$$

3 dB Open-Loop Response

The **open-loop gain** of an op-amp is determined by the internal design and it very high. The high frequency cutoff frequency of an open-loop op-amp is about 10 Hz.

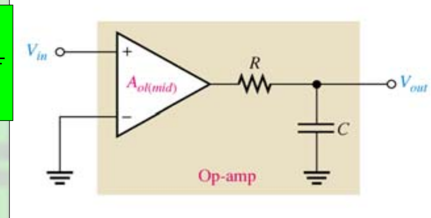


Ideal plot of open-loop voltage gain versus frequency for a typical op-amp. The frequency scale is logarithmic.

Open-Loop Frequency Response

The internal RC circuit of an op-amp limits the gain at frequencies higher than the cutoff frequency. The gain of an open-loop op-amp can be determined at any frequency by the formula below.

$$A_{ol} = \frac{A_{ol(mid)}}{\sqrt{1 + f^2/f_c^2}}$$



Op-amp represented by a gain element and an internal RC circuit.

Ex 12–13 Determine A_{ol} for the following values of *f*.
Assume $f_{c(ol)} = 100$ Hz and $A_{ol(mid)} = 100{,}000$.
(a) *f* = 0 Hz (b) *f* = 10 Hz (c) *f* = 100 Hz (d) *f* = 1000 Hz

$$(a)\quad A_{ol} = \frac{A_{ol(mid)}}{\sqrt{1+f^2/f_{c(cl)}^2}} = \frac{100{,}000}{\sqrt{1+0}} = 100{,}000$$

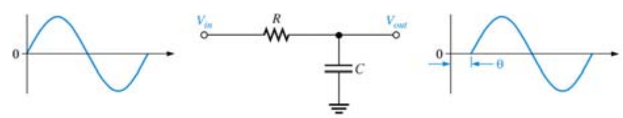
$$(b)\quad A_{ol} = \frac{100{,}000}{\sqrt{1+(0.1)^2}} = 99{,}503$$

$$(c)\quad A_{ol} = \frac{100{,}000}{\sqrt{1+(1)^2}} = 70{,}710$$

$$(d)\quad A_{ol} = \frac{100{,}000}{\sqrt{1+(10)^2}} = 9950$$

Open-Loop Response – Phase Shift

Of course as with any RC circuit phase shift begins to occur at higher frequencies. Remember we are viewing internal characteristics as external components.



$$Phase\ Shift\ (\theta) = -\tan^{-1}\left(\frac{f}{f_c}\right)$$

Ex 12–14 Calculate the phase shift for an RC lag circuit for each of the following frequencies, and then the curve of phase shift versus frequency. Assume $f_c = 100$ Hz
(a) *f* = 1 Hz (b) *f* = 10 Hz (c) *f* = 100 Hz (d) *f* = 1000 Hz (e) *f* = 10,000 Hz

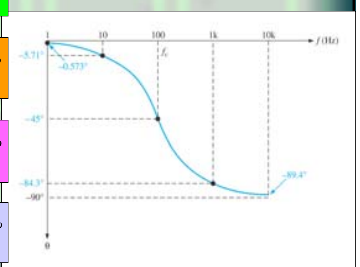
$$(a)\quad \theta = -\tan^{-1}\left(\frac{f}{f_c}\right) = -\tan^{-1}\left(\frac{1\,Hz}{100\ Hz}\right) = -0.573^\circ$$

$$(b)\quad \theta = -\tan^{-1}\left(\frac{10\ Hz}{100\ Hz}\right) = -5.71^\circ$$

$$(c)\quad \theta = -\tan^{-1}\left(\frac{100\ Hz}{100\ Hz}\right) = -45^\circ$$

$$(d)\quad \theta = -\tan^{-1}\left(\frac{1000\ Hz}{100\ Hz}\right) = -84.3^\circ$$

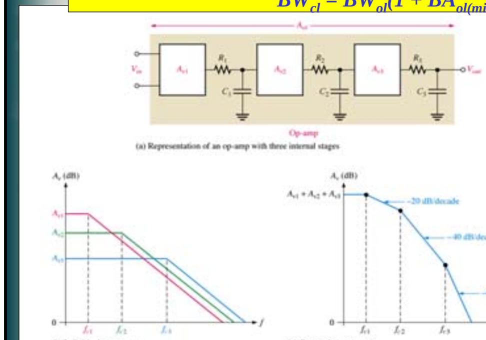
$$(e)\quad \theta = -\tan^{-1}\left(\frac{10{,}000\ Hz}{100\ Hz}\right) = -89.4^\circ$$



Closed-Loop Response

Op-amps are normally used in a closed loop configuration with negative feedback. While the gain reduced the bandwidth is increased. The bandwidth (BW) of a closed-loop op-amp can be determined by the formula below. Remember *B* is the feedback attenuation.

$$BW_{cl} = BW_{ol}(1 + BA_{ol(mid)})$$



$$\theta_{tot} = -\tan^{-1}\left(\frac{f}{f_{c1}}\right) - \tan^{-1}\left(\frac{f}{f_{c2}}\right) - \tan^{-1}\left(\frac{f}{f_{c3}}\right)$$

Ex 12–15 A certain op-amp has three internal amplifier stages with the following gains and critical frequencies:

Stage 1: A_{v1} = 40 dB, f_{c1} = 2 kHz

Stage 2: A_{v2} = 32 dB, f_{c2} = 40 kHz

Stage 3: A_{v3} = 20 dB, f_{c3} = 150 kHz

Determine the open-loop midrange gain in decibels and the total phase lag when $f = f_{c1}$

$A_{ol(mid)} = A_{v1} + A_{v2} + A_{v3}$ = 40 dB + 32 dB + 20 dB = 92 dB

$$\theta_{tot} = -\tan^{-1}\left(\frac{f}{f_{c1}}\right) - \tan^{-1}\left(\frac{f}{f_{c2}}\right) - \tan^{-1}\left(\frac{f}{f_{c3}}\right)$$

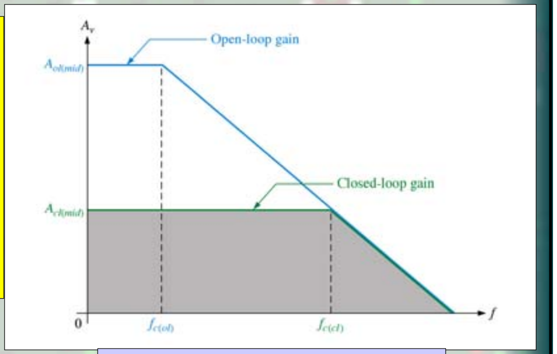
$$= -\tan^{-1}(1) - \tan\left(\frac{2}{40}\right) - \tan\left(\frac{2}{150}\right)$$

$$= -45^\circ - 2.86^\circ - 0.76^\circ$$

$$= -48.6^\circ$$

Closed-Loop Response

The **gain-bandwidth product** is always equal to the frequency at which the op-amp's open-loop gain is 0dB (unity-gain bandwidth).



Closed-loop gain compared to open-loop gain.

$BW_{cl} = BW_{ol}(1 + BA_{ol(mid)})$