

NEW YORK CITY COLLEGE OF TECHNOLOGY
The City University of New York

DEPARTMENT: Electrical Engineering Technology

SUBJECT CODE EET2162/ET382
AND TITLE: Digital Electronics I

COURSE DESCRIPTION: Fundamental of digital electronics using Boolean algebra, truth tables, Karnaugh maps and waveforms to analyze and understand digital logic circuit design. Logic gates (AND, OR, NOR, EX-OR), binary arithmetic, flip-flops, counters and registers are analyzed in experiments.

PREREQUISITES: EET1240/ET212, EET1241/ET252

TEXTBOOK: Digital Systems Principles and Applications
By Tocci, Widmer, and Moss
Prentice Hall 2006

**COURSE OBJECTIVES/
COURSE OUTCOMES:**

1. Upon completion of this course students will be able to: Analyze and design combinatorial logic circuits with multiple inputs or outputs (ABET Criteria, 2a, 2b, 2c, 2d, 2e, 2f, 2k)
2. Use Boolean algebra and Kmapping to reduce logic hardware to a minimum number of gates. (ABET Criteria 2a, 2b, 2c, 2d, 2f, 2k).
3. Convert logic circuits to NAND or NOR logic (ABET Criteria 2a, 2c, 2d, 2f, 2k).
4. Analyze and design arithmetic circuits. (ABET Criteria 2a, 2b, 2c, 2d, 2e, 2f, 2k).
5. Analyze and design sequential logic circuits with multiple inputs/outputs (ABET Criteria 2a, 2b, 2c, 2d, 2e, 2f, 2k).
6. Analyze and design counters and registers (ABET Criteria 2a, 2b, 2c, 2d, 2e, 2f, 2k).

TOPICS: Topics include analysis, design implementation, and testing of basic combinatorial and sequential logic circuits: Boolean algebra, and Karnaugh mapping techniques are covered to reduce redundant hardware.

CLASS HOURS: 2

LAB HOURS: 3

CREDITS: 3

Prepared by: Professors K. Markowitz/November 2006

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EXPERIMENTS ET2162/ET382

WEEK

1	Orientation & Pulse Measurements.
2	Limiting and Clipping Circuits.
3	Pilot Ejection and 3 Voter Problem Using the Digiac.
4	Binary-Decimal and Decimal-Binary Decoders using the Digiac.
5	Combinational Lock using the Digiac.
6	Automatic Control using the Digiac.
7	Flip-Flops, Counting Circuits and Displays using the Digiac.
8	Mid-Semester Exam.
9	Combinational Logic using the SN7400 and Digi Designer.
10	Combinational Logic SN7400 (continued).
11	Sequential Logic using the 7476 and Digi Designer.
12	Counters using the SN7490.
13	Counters, Drivers, and Displays (7490, 7447, CO8708).
14	SN 7486 EX-OR
15	Final Exam

GRADING POLICY:

Homework and class participation	10%
Exam1	20%
Midterm Exam:	20%
Lab Reports	15%
Final Exam	35%

<u>Letter Grade</u>	<u>Numerical Grade Ranges</u>	<u>Quality</u>
A	93-100	4.0
A-	90-92.9	3.7
B+	87-89.9	3.3
B	83-86.9	3.0
B-	80-82.9	2.7
C+	77-79.9	2.3
C	70-76.9	2.0
D	60-69.9	1.0
F	59.9 and below	0.0

WEEK	TOPIC	READING ASSIGNMENT	HOMEWORK
1	Introduction to the course, Comparison of digital vs. analog systems, The binary number system, Digital signals and timing diagram, Parallel vs. serial transmission Binary to decimal conversion, Decimal to binary conversion.	Chapter 1 Textbook: Pages 1-17	Textbook: Pr. 1.1-1-6
2	Octal number system: Octal to decimal conversion, Octal to binary conversion, Binary to octal conversion Hexadecimal number system: Hex to decimal conversion, Hex to binary conversion, Hex to octal conversion Binary Coded Decimal, What is a byte? ASCII code, Parity (even and odd), one bit error detection.	Chapter 2 Textbook: Pages 25-44	Textbook: Pr 2.1-2.6, 2.11, 2.14, 2.20, 2.21, 2.22, and 2.24
3	Logic gates and Boolean algebra AND, OR, INVERTER, gates symbols and truth tables Describing the above gates algebraically; Describing logic circuits algebraically; Implementing circuits from a Boolean expression.	Chapter 3 Textbook: Pages 55-71	Textbook: Pr. 3.1, 3.2, 3.11, 3.12, 3.13, and 3.16
4	Exam 1		
5-6	NAND, NOR, and Exclusive OR gates. Booleans Theorems, De Morgan's Law Conversion of digital circuits to NAND gates only. Conversion of digital circuits to NOR gates only.	Chapter 3 Textbook: Pages 72-96	Textbook: Pr. 3.9, 3.22, 3.24, 3.28, and 3.29
7-8	Sum of products expression Product of sums expression Simplifications of Boolean expressions using Boolean algebra, and Karnaugh maps. Designing combinational logic circuits.	Chapter 4 Textbook: Pages 107-133	Textbook: Pr. 4.1, 4.2, 4.3, 4.5, 4.6, 4.7, 4.8, 4.18, 4.19, 4.22, and 4.23
9	Midterm Examination.		
10	Parity Generator Basic characteristics of IC's (TTL and CMOS) Floating inputs. Trouble shooting digital systems. Exclusive OR gate.	Chapter 4 Textbook: Pages 133-160	
11	Latches and Flip flops, NAND gate Latch Clocked Flip-flops: S-C Flip-flop, J-K Flip-flop, D Flip-flop, T Flip-flop, Timing diagrams. Asynchronous inputs, Input sequence detector circuits	Chapter 5 Textbook: Pages 181-244	Textbook: Pr. 5.8, 5.9, 5.11, 5.12, 5.16, 5.17, and 5.18
12	Shift registers, Counters, One Shot device, Analyzing sequential circuits	Chapter 5 Textbook: Pages 245-260	Textbook: Pr. 5.27, 5.39, 5.31, and 5.32
13	Binary addition signed numbers 1's complement form. 2's complement form; Addition in the 2's complement system; Subtraction in the 2's complement system; Arithmetic circuits, Full adder, Full subtractor.	Chapter 6 Textbook: Pages 298-323	Textbook: Pr. 6.1, 6.5, 6.9, 6.10, 6.18, and 6.19
14	Up-counters; Up-down counters; Down-counters; Shift register	Chapter 7 Textbook: Pages 362-445	
15	Final Examination		